April 2014

# FAN3223 / FAN3224 / FAN3225
# Dual 4-A High-Speed, Low-Side Gate Drivers

## Features

- Industry-Standard Pinouts
- 4.5-V to 18-V Operating Range
- 5-A Peak Sink/Source at $V_{DD}$ = 12 V
- 4.3-A Sink / 2.8-A Source at $V_{OUT}$ = 6 V
- Choice of TTL or CMOS Input Thresholds
- Three Versions of Dual Independent Drivers:
  - Dual Inverting + Enable (FAN3223)
  - Dual Non-Inverting + Enable (FAN3224)
  - Dual-Inputs (FAN3225)
- Internal Resistors Turn Driver Off If No Inputs
- MillerDrive™ Technology
- 12-ns / 9-ns Typical Rise/Fall Times (2.2-nF Load)
- Under 20-ns Typical Propagation Delay Matched within 1 ns to the Other Channel
- Double Current Capability by Paralleling Channels
- 8-Lead 3x3 mm MLP or 8-Lead SOIC Package
- Rated from –40°C to +125°C Ambient
- Automotive Qualified to AEC-Q100 (F085 Version)

## Applications

- Switch-Mode Power Supplies
- High-Efficiency MOSFET Switching
- Synchronous Rectifier Circuits
- DC-to-DC Converters
- Motor Control
- Automotive-Qualified Systems (F085 version)

## Description

The FAN3223-25 family of dual 4 A gate drivers is designed to drive N-channel enhancement-mode MOSFETs in low-side switching applications by providing high peak current pulses during the short switching intervals. The driver is available with either TTL or CMOS input thresholds. Internal circuitry provides an under-voltage lockout function by holding the output LOW until the supply voltage is within the operating range. In addition, the drivers feature matched internal propagation delays between A and B channels for applications requiring dual gate drives with critical timing, such as synchronous rectifiers. This also enables connecting two drivers in parallel to effectively double the current capability driving a single MOSFET.

The FAN322X drivers incorporate MillerDrive™ architecture for the final output stage. This bipolar-MOSFET combination provides high current during the Miller plateau stage of the MOSFET turn-on / turn-off process to minimize switching loss, while providing rail-to-rail voltage swing and reverse current capability.

The FAN3223 offers two inverting drivers and the FAN3224 offers two non-inverting drivers. Each device has dual independent enable pins that default to ON if not connected. In the FAN3225, each channel has dual inputs of opposite polarity, which allows configuration as non-inverting or inverting with an optional enable function using the second input. If one or both inputs are left unconnected, internal resistors bias the inputs such that the output is pulled LOW to hold the power MOSFET OFF.

## Related Resources

*AN-6069 — Application Review and Comparative Evaluation of Low-Side Gate Drivers*

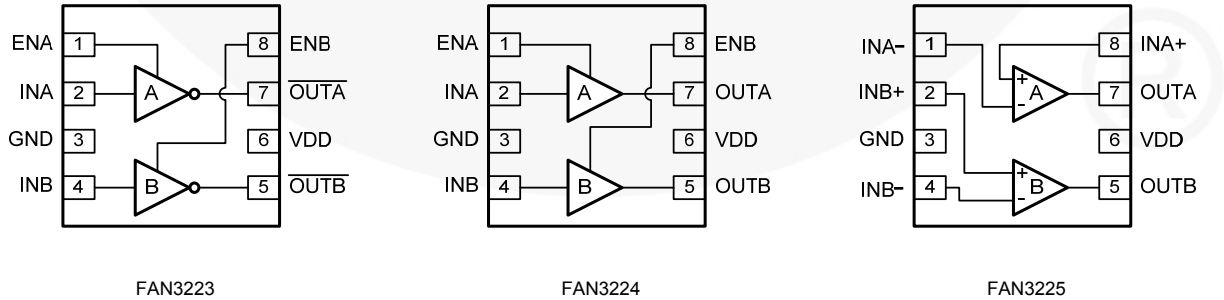


**Figure 1. Pin Configurations**

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## Ordering Information

| Part Number | Logic | Input Threshold | Package | Packing Method | Quantity per Reel |
|---|---|---|---|---|---|
| FAN3223CMPX | Dual Inverting Channels + Dual Enable | CMOS | 3x3 mm MLP-8 | Tape & Reel | 3,000 |
| FAN3223CMX | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3223CMX_F085(1) | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3223TMPX | | TTL | 3x3 mm MLP-8 | Tape & Reel | 3,000 |
| FAN3223TMX | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3223TMX_F085(1) | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3224CMPX | Dual Non-Inverting Channels + Dual Enable | CMOS | 3x3 mm MLP-8 | Tape & Reel | 3,000 |
| FAN3224CMX | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3224CMX_F085(1) | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3224TMPX | | TTL | 3x3 mm MLP-8 | Tape & Reel | 3,000 |
| FAN3224TMX | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3224TMX_F085(1) | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3225CMPX | Dual Channels of Two-Input / One-Output Drivers | CMOS | 3x3 mm MLP-8 | Tape & Reel | 3,000 |
| FAN3225CMX | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3225CMX_F085(1) | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3225TMPX | | TTL | 3x3 mm MLP-8 | Tape & Reel | 3,000 |
| FAN3225TMX | | | SOIC-8 | Tape & Reel | 2,500 |
| FAN3225TMX_F085(1) | | | SOIC-8 | Tape & Reel | 2,500 |

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**Note:**

1. Qualified to AEC-Q100.

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## Package Outlines

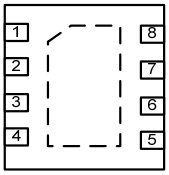


**Figure 2. 3x3 mm MLP-8 (Top View)**

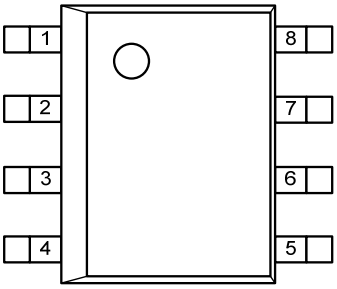


**Figure 3. SOIC-8 (Top View)**

## Thermal Characteristics[2]

| Package | $\Theta_{JL}$[3] | $\Theta_{JT}$[4] | $\Theta_{JA}$[5] | $\Psi_{JB}$[6] | $\Psi_{JT}$[7] | Units |
|---|---|---|---|---|---|---|
| 8-Lead 3x3 mm Molded Leadless Package (MLP) | 1.2 | 64 | 42 | 2.8 | 0.7 | °C/W |
| 8-Pin Small Outline Integrated Circuit (SOIC) | 38 | 29 | 87 | 41 | 2.3 | °C/W |

**Notes:**

2. Estimates derived from thermal simulation; actual values depend on the application.
3. Theta_JL ($\Theta_{JL}$): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
4. Theta_JT ($\Theta_{JT}$): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top-side heatsink.
5. Theta_JA ($\Theta_{JA}$): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink using a 2S2P board, as specified in JEDEC standards JESD51-2, JESD51-5, and JESD51-7, as appropriate.
6. Psi_JB ($\Psi_{JB}$): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 5. For the MLP-8 package, the board reference is defined as the PCB copper connected to the thermal pad and protruding from either end of the package. For the SOIC-8 package, the board reference is defined as the PCB copper adjacent to pin 6.
7. Psi_JT ($\Psi_{JT}$): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 5.

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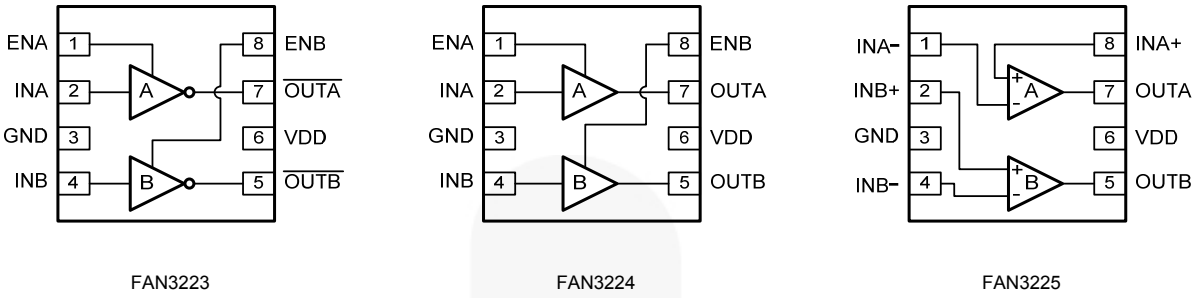


FAN3223 FAN3224 FAN3225

**Figure 4. Pin Assignments (Repeated)**

## Pin Definitions

| Name | Pin Description |
|---|---|
| ENA | **Enable Input for Channel A**. Pull pin LOW to inhibit driver A. ENA has TTL thresholds for both TTL and CMOS INx threshold. |
| ENB | **Enable Input for Channel B**. Pull pin LOW to inhibit driver B. ENB has TTL thresholds for both TTL and CMOS INx threshold. |
| GND | **Ground**. Common ground reference for input and output circuits. |
| INA | **Input to Channel A**. |
| INA+ | **Non-Inverting Input to Channel A**. Connect to VDD to enable output. |
| INA- | **Inverting Input to Channel A**. Connect to GND to enable output. |
| INB | **Input to Channel B**. |
| INB+ | **Non-Inverting Input to Channel B**. Connect to VDD to enable output. |
| INB- | **Inverting Input to Channel B**. Connect to GND to enable output. |
| OUTA | **Gate Drive Output A**: Held LOW unless required input(s) are present and $V_{DD}$ is above UVLO threshold. |
| OUTB | **Gate Drive Output B**: Held LOW unless required input(s) are present and $V_{DD}$ is above UVLO threshold. |
| $\overline{\text{OUTA}}$ | **Gate Drive Output A** (inverted from the input): Held LOW unless required input is present and $V_{DD}$ is above UVLO threshold. |
| $\overline{\text{OUTB}}$ | **Gate Drive Output B** (inverted from the input): Held LOW unless required input is present and $V_{DD}$ is above UVLO threshold. |
| P1 | **Thermal Pad** (MLP only). Exposed metal on the bottom of the package; may be left floating or connected to GND; NOT suitable for carrying current. |
| VDD | **Supply Voltage**. Provides power to the IC. |

## Output Logic

| FAN3223 (x=A or B) | | |
|---|---|---|
| **ENx** | **INx** | **$\overline{\text{OUTx}}$** |
| 0 | 0 | 0 |
| 0 | 1(8) | 0 |
| 1(8) | 0 | 1 |
| 1(8) | 1(8) | 0 |

| FAN3224 (x=A or B) | | |
|---|---|---|
| **ENx** | **INx** | **OUTx** |
| 0 | 0(8) | 0 |
| 0 | 1 | 0 |
| 1(8) | 0(8) | 0 |
| 1(8) | 1 | 1 |

| FAN3225 (x=A or B) | | |
|---|---|---|
| **INx+** | **INx−** | **OUTx** |
| 0(8) | 0 | 0 |
| 0(8) | 1(8) | 0 |
| 1 | 0 | 1 |
| 1 | 1(8) | 0 |

**Note:**
8. Default input signal if no external connection is made.

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## Block Diagrams

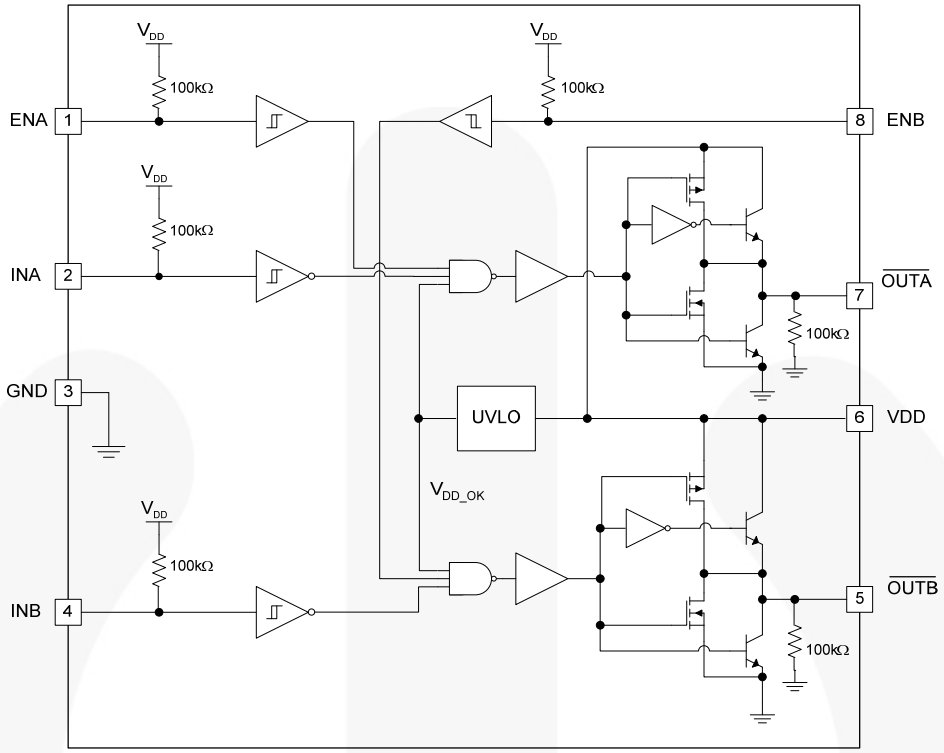


**Figure 5. FAN3223 Block Diagram**

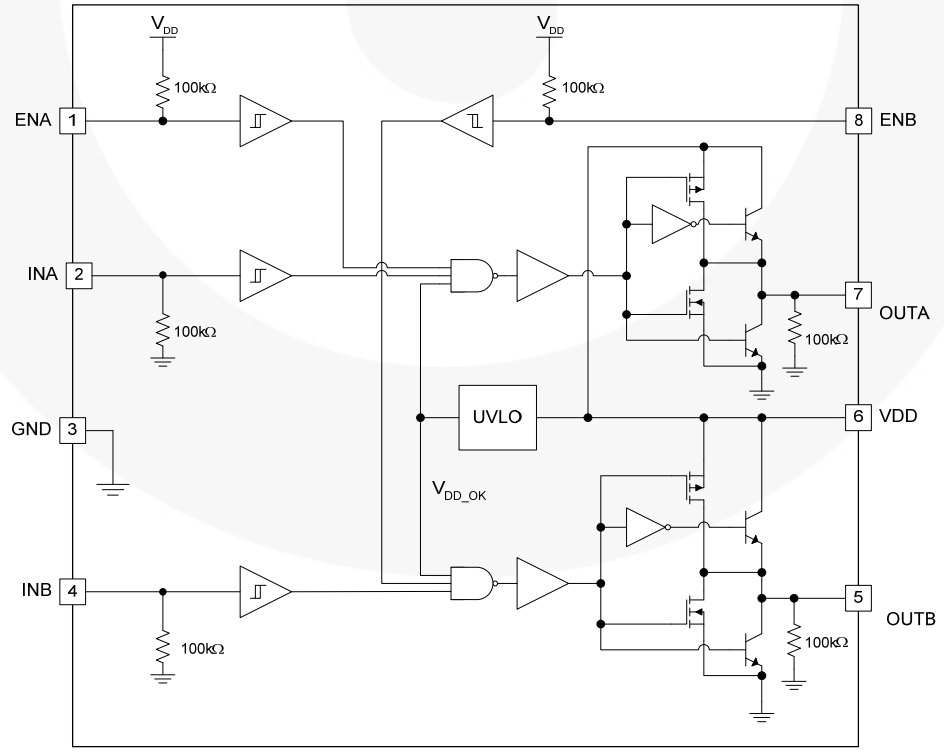


**Figure 6. FAN3224 Block Diagram**

## Block Diagrams

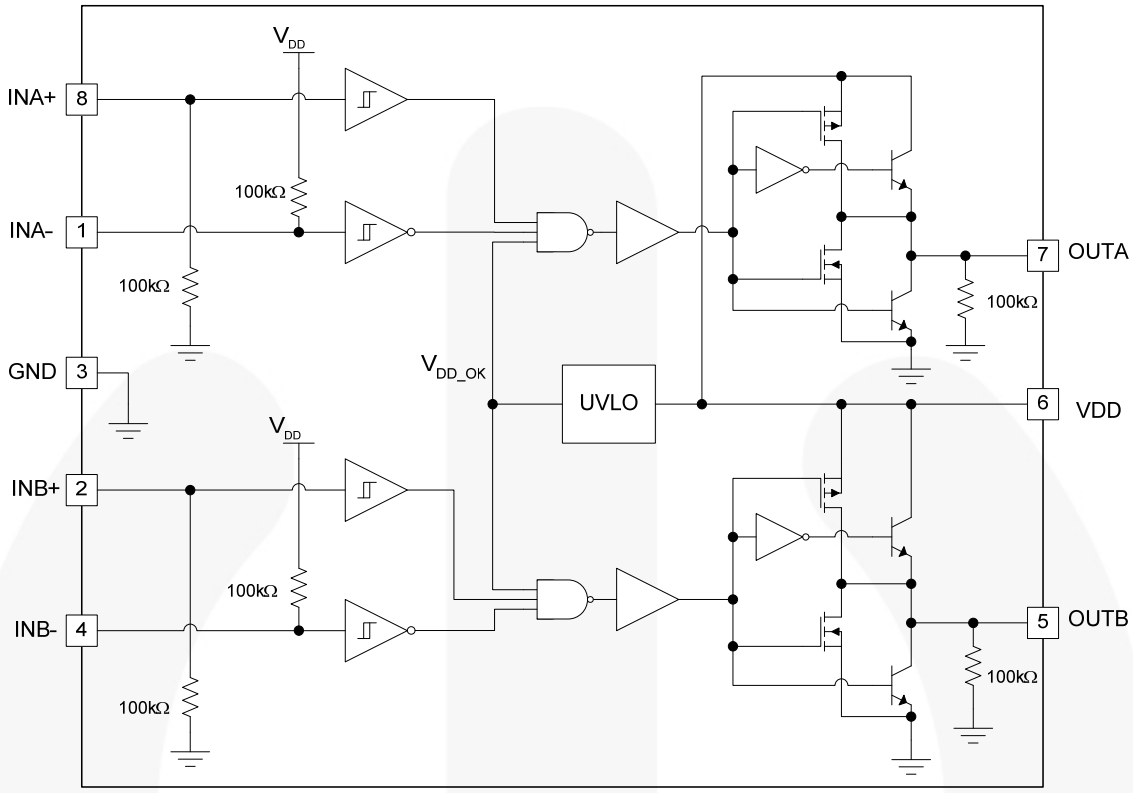


**Figure 7. FAN3225 Block Diagram**

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | VDD to PGND | | -0.3 | 20.0 | V |
| $V_{EN}$ | ENA and ENB to GND | | GND - 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{IN}$ | INA, INA+, INA–, INB, INB+ and INB– to GND | | GND - 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{OUT}$ | OUTA and OUTB to GND | DC | GND - 0.3 | $V_{DD}$ + 0.3 | V |
| $T_L$ | Lead Soldering Temperature (10 Seconds) | | | +260 | ºC |
| $T_J$ | Junction Temperature | | -55 | +150 | ºC |
| $T_{STG}$ | Storage Temperature | | -65 | +150 | ºC |

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage Range | | 4.5 | 18.0 | V |
| $V_{EN}$ | Enable Voltage ENA and ENB | | 0 | $V_{DD}$ | V |
| $V_{IN}$ | Input Voltage INA, INA+, INA–, INB, INB+ and INB– | | 0 | $V_{DD}$ | V |
| $V_{OUT}$ | OUTA and OUTB to GND | Repetitive Pulse < 200 ns | -2.0 | $V_{DD}$ + 0.3 | V |
| $T_A$ | Operating Ambient Temperature | | -40 | +125 | ºC |

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## Electrical Characteristics

Unless otherwise noted, $V_{DD}$=12 V, $T_J$=-40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{DD}$ | Operating Range | | 4.5 | | 18.0 | V |
| $I_{DD}$ | Supply Current, Inputs / EN Not Connected | All except FAN3225C | | 0.70 | 0.95 | mA |
| | | FAN3225C(9) | | 0.21 | 0.35 | mA |
| $V_{ON}$ | Turn-On Voltage | INA=ENA=$V_{DD}$, INB=ENB=0 V | 3.5 | 3.9 | 4.3 | V |
| $V_{OFF}$ | Turn-Off Voltage | INA=ENA=$V_{DD}$, INB=ENB=0 V | 3.3 | 3.7 | 4.1 | V |
| **FAN322xTMX_F085, FAN322xCMX_F085 (Automotive-Qualified Versions)** | | | | | | |
| $V_{DD}$ | Operating Range | | 4.5 | | 18.0 | V |
| $I_{DD}$ | Supply Current, Inputs / EN Not Connected(14) | All Except FAN3225C | | 0.70 | 1.20 | mA |
| | | FAN3225C(9) | | 0.21 | 0.35 | mA |
| $V_{ON}$ | Turn-On Voltage(14) | INA=ENA=$V_{DD}$, INB=ENB=0 V | 3.4 | 3.9 | 4.5 | V |
| $V_{OFF}$ | Turn-Off Voltage(14) | INA=ENA=$V_{DD}$, INB=ENB=0 V | 3.2 | 3.7 | 4.3 | V |
| **Inputs (FAN322xT)(10)** | | | | | | |
| $V_{INL_T}$ | INx Logic LOW Threshold | | 0.8 | 1.2 | | V |
| $V_{INH_T}$ | INx Logic HIGH Threshold | | | 1.6 | 2.0 | V |
| $V_{HYS_T}$ | TTL Logic Hysteresis Voltage | | 0.2 | 0.4 | 0.8 | V |
| $I_{IN+}$ | Non-Inverting Input Current | IN from 0 to $V_{DD}$ | -1 | | 175 | µA |
| $I_{IN-}$ | Inverting Input Current | IN from 0 to $V_{DD}$ | -175 | | 1 | µA |
| **FAN322xTMX_F085 (Automotive-Qualified Versions)** | | | | | | |
| $V_{INL_T}$ | INx Logic LOW Threshold | | 0.8 | 1.2 | | V |
| $V_{INH_T}$ | INx Logic HIGH Threshold | | | 1.6 | 2.0 | V |
| $V_{HYS_T}$ | TTL Logic Hysteresis Voltage | | 0.1 | 0.4 | 0.9 | V |
| $I_{INx_T}$ | Non-inverting Input Current(14) | IN=0 V | -1.5 | | 1.5 | µA |
| $I_{INx_T}$ | Non-inverting Input Current(14) | IN=$V_{DD}$ | 90 | 120 | 175 | µA |
| $I_{INx_T}$ | Inverting Input Current(14) | IN=0 V | -175 | -120 | -90 | µA |
| $I_{INx_T}$ | Inverting Input Current(14) | IN=$V_{DD}$ | -1.5 | | 1.5 | µA |
| **Inputs (FAN322xC)(10)** | | | | | | |
| $V_{INL_C}$ | INx Logic Low Threshold | | 30 | 38 | | %$V_{DD}$ |
| $V_{INH_C}$ | INx Logic High Threshold | | | 55 | 70 | %$V_{DD}$ |
| $V_{HYS_C}$ | CMOS Logic Hysteresis Voltage | | | 17 | | %$V_{DD}$ |
| $I_{IN+}$ | Non-Inverting Input Current | IN from 0 to $V_{DD}$ | -1 | | 175 | µA |
| $I_{IN-}$ | Inverting Input Current | IN from 0 to $V_{DD}$ | -175 | | 1 | µA |

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## Electrical Characteristics

Unless otherwise noted, $V_{DD}$=12 V, $T_J$=-40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **FAN322xCMX_F085 (Automotive-Qualified Versions)** | | | | | | |
| $V_{INL_C}$ | INx Logic Low Threshold | | 30 | 38 | | %$V_{DD}$ |
| $V_{INH_C}$ | INx Logic High Threshold | | | 55 | 70 | %$V_{DD}$ |
| $V_{HYS_C}$ | CMOS Logic Hysteresis Voltage | | | 17 | | %$V_{DD}$ |
| $I_{INx_T}$ | Non-Inverting Input Current(14) | IN=0 V | -1.5 | | 1.5 | µA |
| $I_{INx_T}$ | Non-Inverting Input Current(14) | IN=$V_{DD}$ | 90 | 120 | 175 | µA |
| $I_{INx_T}$ | Inverting Input Current(14) | IN=0 V | -175 | -120 | -90 | µA |
| $I_{INx_T}$ | Inverting Input Current(14) | IN=$V_{DD}$ | -1.5 | | 1.5 | µA |
| **ENABLE (FAN3223C, FAN3223T, FAN3224C, FAN3224T)** | | | | | | |
| $V_{ENL}$ | Enable Logic Low Threshold | EN from 5 V to 0 V | 0.8 | 1.2 | | V |
| $V_{ENH}$ | Enable Logic High Threshold | EN from 0 V to 5 V | | 1.6 | 2.0 | V |
| $V_{HYS_T}$ | TTL Logic Hysteresis Voltage(11) | | | 0.4 | | V |
| $R_{PU}$ | Enable Pull-Up Resistance(11) | | | 100 | | kΩ |
| $t_{D3}$ | EN to Output Propagation Delay(12) | 0 V to 5 V EN, 1 V/ns Slew Rate | 9 | 17 | 26 | ns |
| $t_{D4}$ | | 5 V to 0 V EN, 1 V/ns Slew Rate | 11 | 18 | 28 | ns |
| **FAN3223C/TMX_F085, FAN3224C/TMX_F085 (Automotive-Qualified Versions)** | | | | | | |
| $V_{ENL}$ | Enable Logic Low Threshold | EN from 5 V to 0 V | 0.8 | 1.2 | | V |
| $V_{ENH}$ | Enable Logic High Threshold | EN from 0 V to 5 V | | 1.6 | 2.0 | V |
| $V_{HYS_T}$ | TTL Logic Hysteresis Voltage(11) | | | 0.4 | | V |
| $R_{PU}$ | Enable Pull-Up Resistance(11) | | | 100 | | kΩ |
| $t_{D3}$ | EN to Output Propagation Delay(12,14) | 0 V to 5V EN, 1 V/ns Slew Rate | 9 | 17 | 34 | ns |
| $t_{D4}$ | | 5 V to 0V EN, 1 V/ns Slew Rate | 9 | 19 | 31 | ns |
| **Outputs** | | | | | | |
| $I_{SINK}$ | OUT Current, Mid-Voltage, Sinking(11) | OUT at $V_{DD}$/2, $C_{LOAD}$=0.22 µF, f=1 kHz | | 4.3 | | A |
| $I_{SOURCE}$ | OUT Current, Mid-Voltage, Sourcing(11) | OUT at $V_{DD}$/2, $C_{LOAD}$=0.22 µF, f=1 kHz | | -2.8 | | A |
| $I_{PK_SINK}$ | OUT Current, Peak, Sinking(11) | $C_{LOAD}$=0.22 µF, f=1 kHz | | 5 | | A |
| $I_{PK_SOURCE}$ | OUT Current, Peak, Sourcing(11) | $C_{LOAD}$=0.22 µF, f=1 kHz | | -5 | | A |
| $t_{RISE}$ | Output Rise Time(13) | $C_{LOAD}$=2200 pF | | 12 | 20 | ns |
| $t_{FALL}$ | Output Fall Time(13) | $C_{LOAD}$=2200 pF | | 9 | 17 | ns |
| $t_{DEL.MATCH}$ | Propagation Matching Between Channels | INA=INB, OUTA and OUTB at 50% Point | | 2 | 4 | ns |
| $I_{RVS}$ | Output Reverse Current Withstand(11) | | | 500 | | mA |
| $t_{D1}$, $t_{D2}$ | Output Propagation Delay, CMOS Inputs(13) | 0 – 12 $V_{IN}$, 1 V/ns Slew Rate | 10 | 18 | 29 | ns |
| $t_{D1}$, $t_{D2}$ | Output Propagation Delay, TTL Inputs(13) | 0 – 5 $V_{IN}$, 1 V/ns Slew Rate | 9 | 17 | 29 | ns |

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## Electrical Characteristics

Unless otherwise noted, $V_{DD}$=12 V, $T_J$=-40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **All Except for FAN3225C/TMX_F085 (Automotive-Qualified Versions)** | | | | | | |
| $t_{RISE}$ | Output Rise Time[13] | $C_{LOAD}$=2200 pF | | 12 | 20 | ns |
| $t_{FALL}$ | Output Fall Time[13] | $C_{LOAD}$=2200 pF | | 9 | 17 | ns |
| $t_{DEL.MATCH}$ | Propagation Matching Between Channels | INA=INB, OUTA and OUTB at 50% Point | | 2 | 4 | ns |
| $I_{RVS}$ | Output Reverse Current Withstand[11] | | | 500 | | mA |
| $t_{D1}$, $t_{D2}$ | Output Propagation Delay, CMOS Inputs[13,14] | 0 – 12 $V_{IN}$, 1 V/ns Slew Rate | 9 | 18 | 34 | ns |
| $t_{D1}$, $t_{D2}$ | Output Propagation Delay, TTL Inputs[13,14] | 0 – 5 $V_{IN}$, 1 V/ns Slew Rate | 6 | 16 | 30 | ns |
| $V_{OH}$ | High Level Output Voltage[14] | $V_{OH}$ =$V_{DD}$–$V_{OUT}$, $I_{OUT}$=–1 mA | | 15 | 35 | mV |
| $V_{OL}$ | Low Level Output Voltage[14] | $I_{OUT}$ = 1 mA | | 10 | 25 | mV |
| **FAN3225C/TMX_F085 (Automotive-Qualificed Versions)** | | | | | | |
| $t_{RISE}$ | Output Rise Time[13] | $C_{LOAD}$=2200 pF | | 12 | 28 | ns |
| $t_{FALL}$ | Output Fall Time[13] | $C_{LOAD}$=2200 pF | | 9 | 26 | ns |
| $V_{OH}$ | High Level Output Voltage[14] | $V_{OH}$ =$V_{DD}$–$V_{OUT}$, $I_{OUT}$=–1 mA | | 15 | 37 | mV |
| $V_{OL}$ | Low Level Output Voltage[14] | $I_{OUT}$ = 1 mA | | 10 | 25 | mV |

**Notes:**

9. Lower supply current due to inactive TTL circuitry.
10. EN inputs have TTL thresholds; refer to the ENABLE section.
11. Not tested in production.
12. *See Timing Diagrams of Figure 10 and Figure 11*.
13. *See Timing Diagrams of Figure 8 and Figure 9.*
14. Applies only to _F085 versions.

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## Timing Diagrams

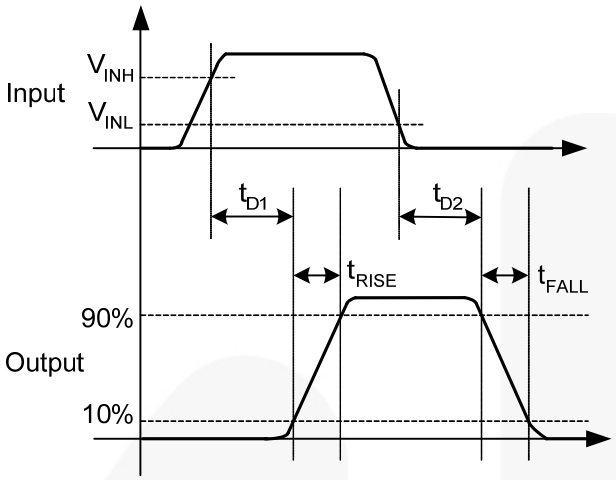


**Figure 8. Non-Inverting (EN HIGH or Floating)**

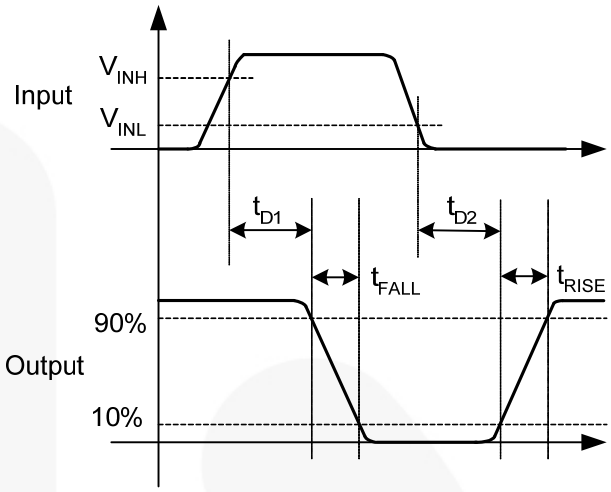


**Figure 9. Inverting (EN HIGH or Floating)**

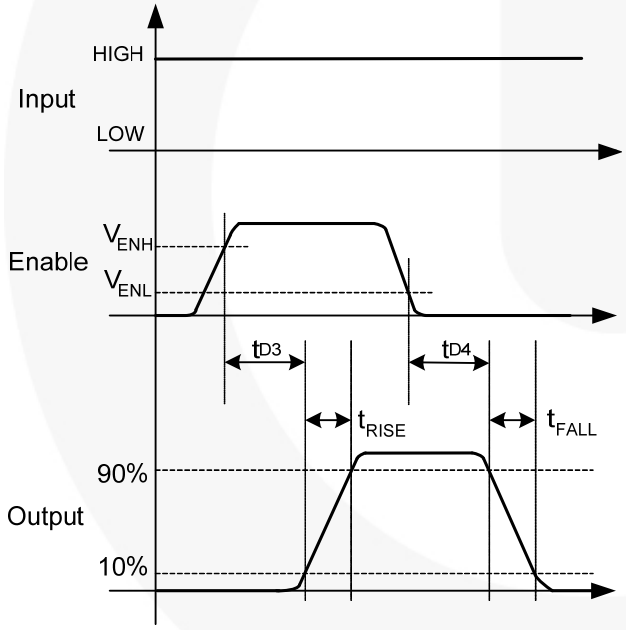


**Figure 10. Non-Inverting (IN HIGH)**

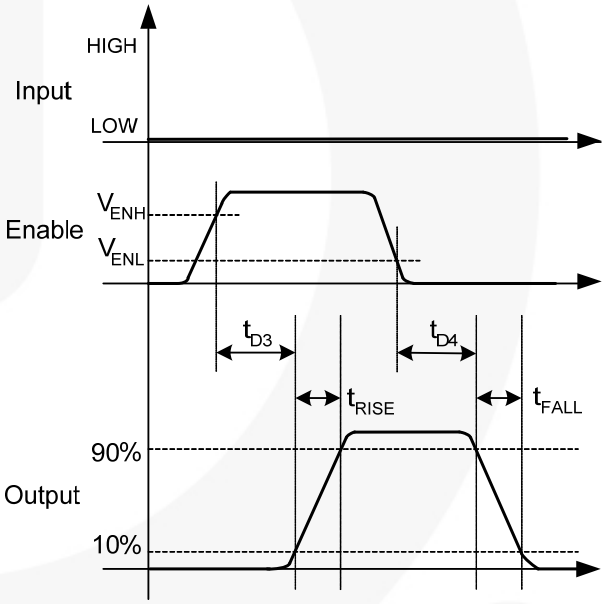


**Figure 11. Inverting (IN LOW)**

## Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}$=12 V unless otherwise noted.

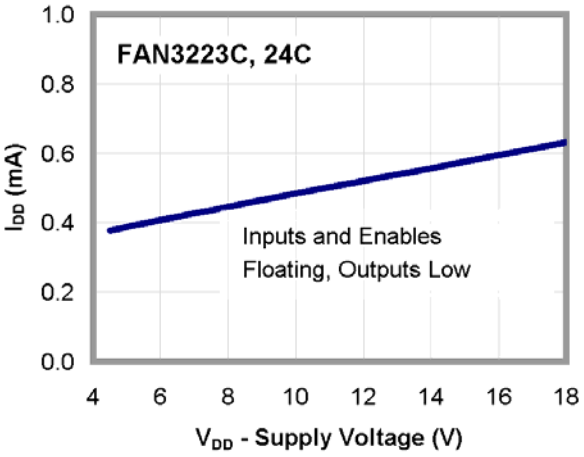


**Figure 12. $I_{DD}$ (Static) vs. Supply Voltage**[15]

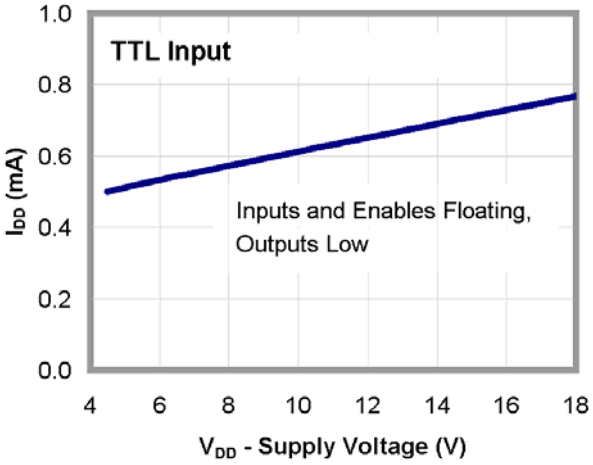


**Figure 13. $I_{DD}$ (Static) vs. Supply Voltage**[15]

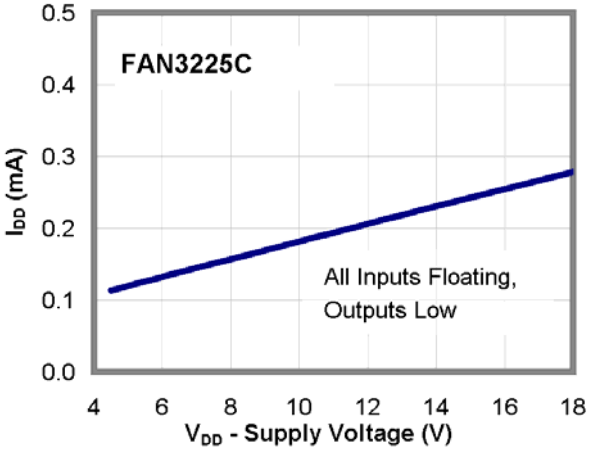


**Figure 14. $I_{DD}$ (Static) vs. Supply Voltage**[15]

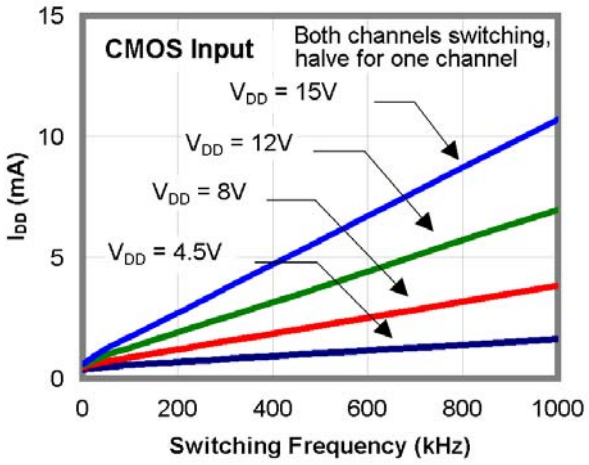


**Figure 15. $I_{DD}$ (No-Load) vs. Frequency**

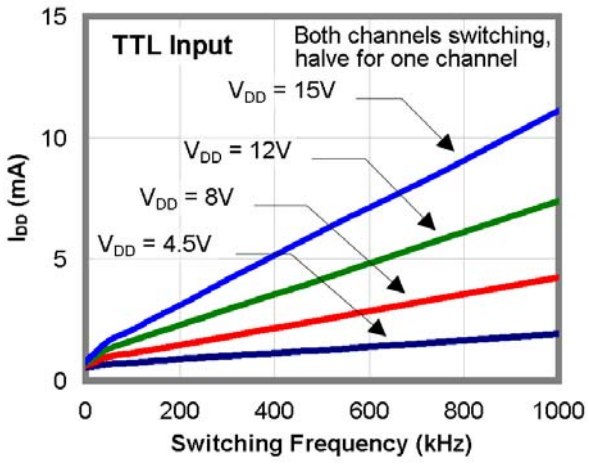


**Figure 16. $I_{DD}$ (No-Load) vs. Frequency**

## Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}$=12 V unless otherwise noted.

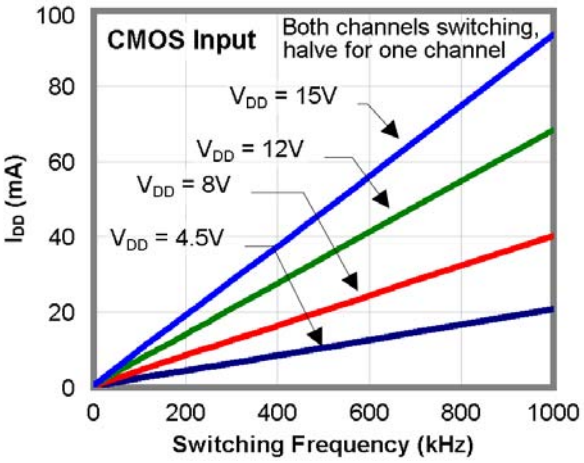


**Figure 17. $I_{DD}$ (2.2 nF Load) vs. Frequency**

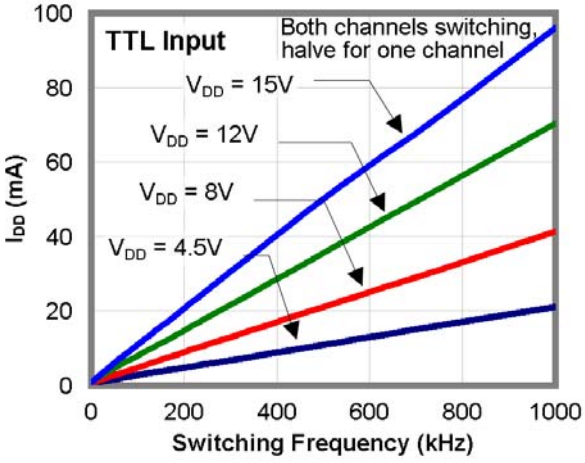


**Figure 18. $I_{DD}$ (2.2 nF Load) vs. Frequency**

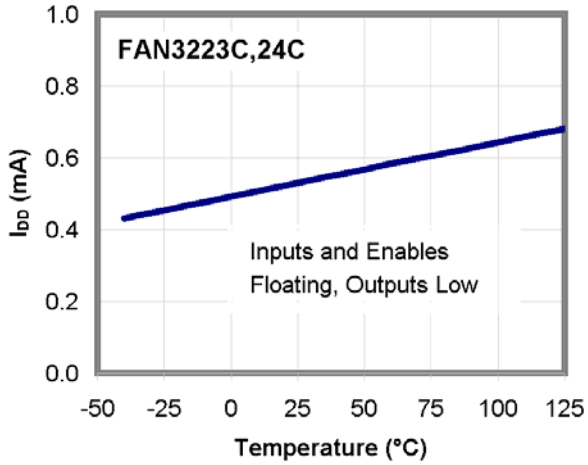


**Figure 19. $I_{DD}$ (Static) vs. Temperature(15)**

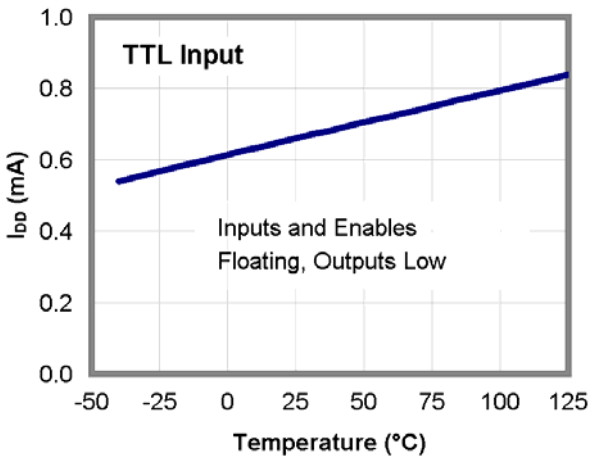


**Figure 20. $I_{DD}$ (Static) vs. Temperature(15)**

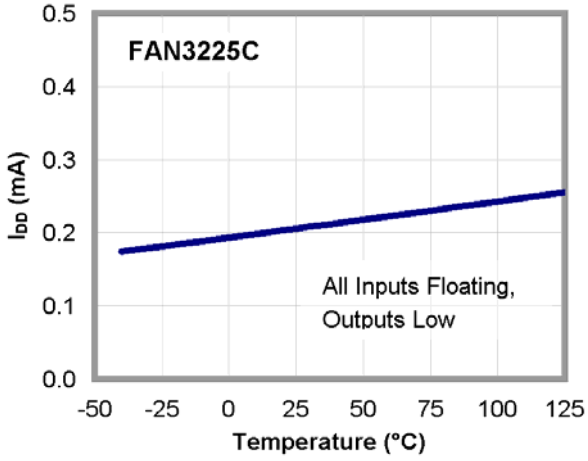


**Figure 21. $I_{DD}$ (Static) vs. Temperature(15)**

## Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}$=12 V unless otherwise noted.

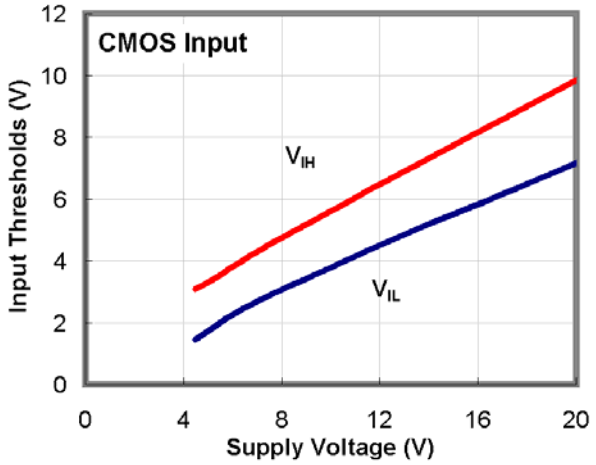


**Figure 22. Input Thresholds vs. Supply Voltage**

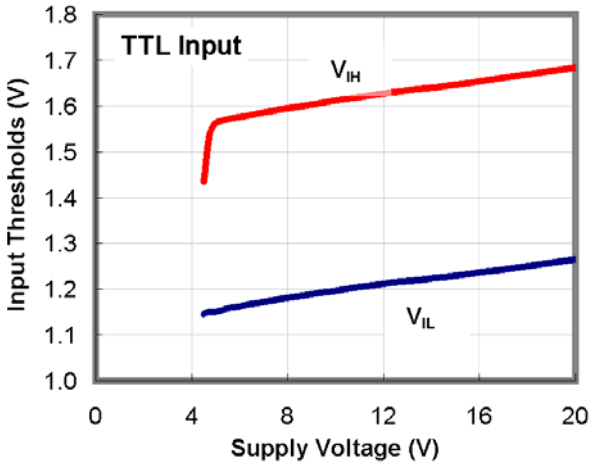


**Figure 23. Input Thresholds vs. Supply Voltage**

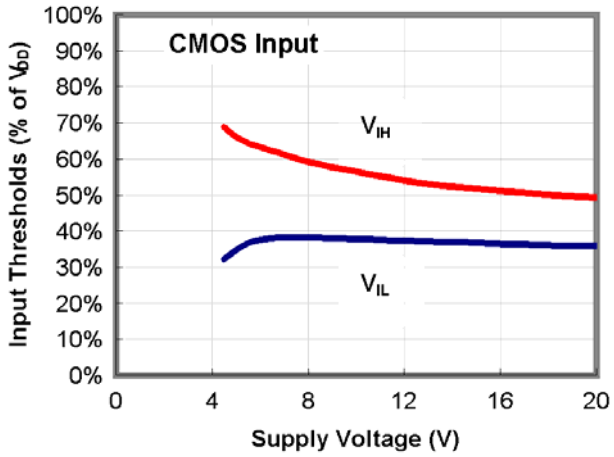


**Figure 24. Input Threshold % vs. Supply Voltage**

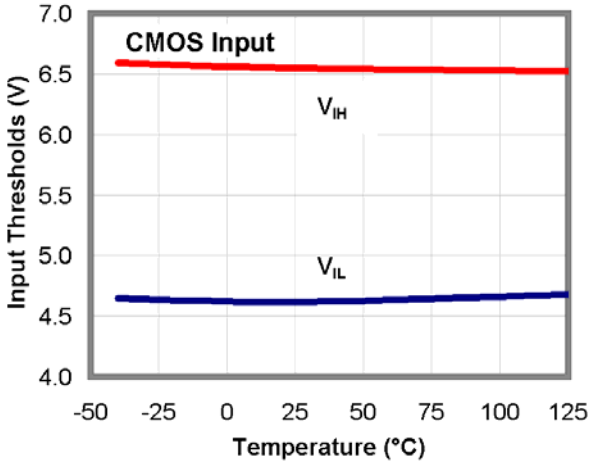


**Figure 25. Input Thresholds vs. Temperature**

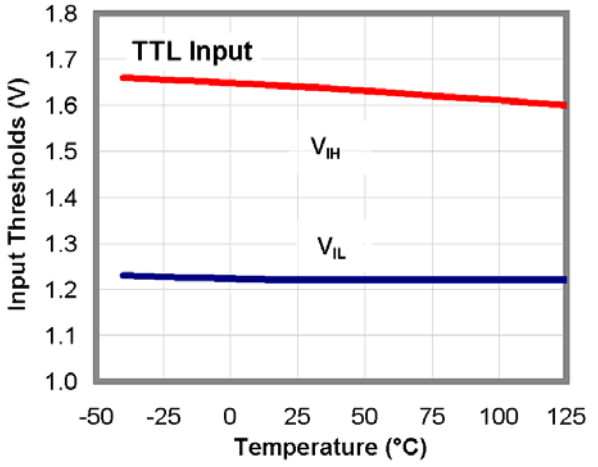


**Figure 26. Input Thresholds vs. Temperature**

## Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}$=12 V unless otherwise noted.

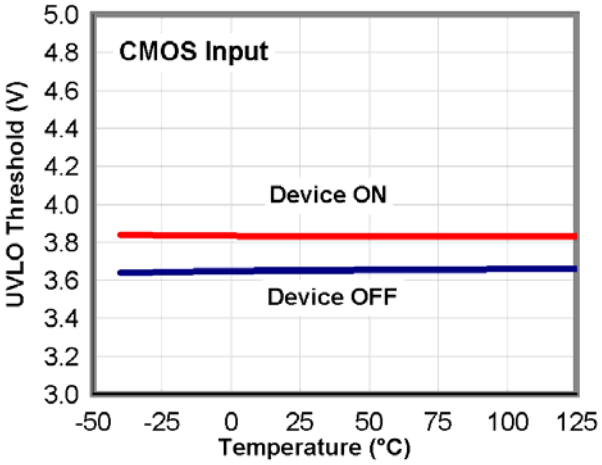


**Figure 27. UVLO Thresholds vs. Temperature**

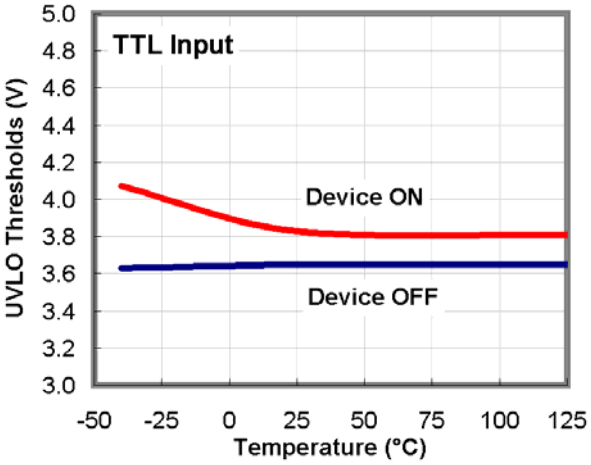


**Figure 28. UVLO Threshold vs. Temperature**

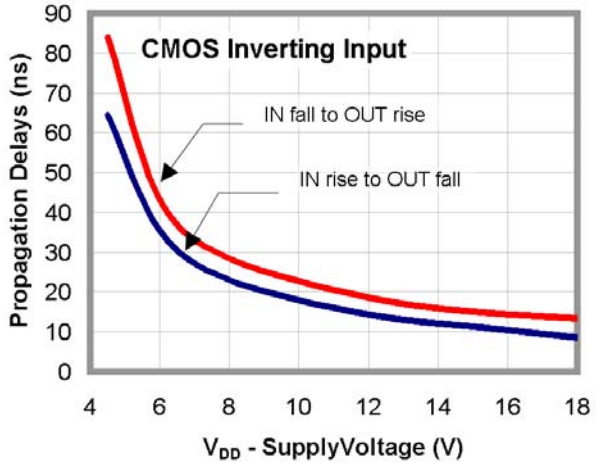


**Figure 29. Propagation Delay vs. Supply Voltage**

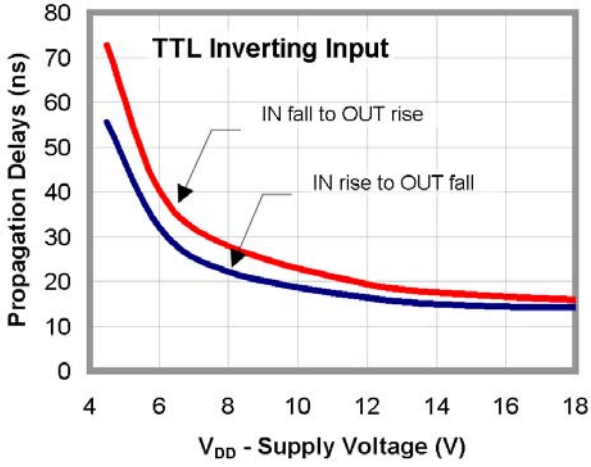


**Figure 30. Propagation Delay vs. Supply Voltage**

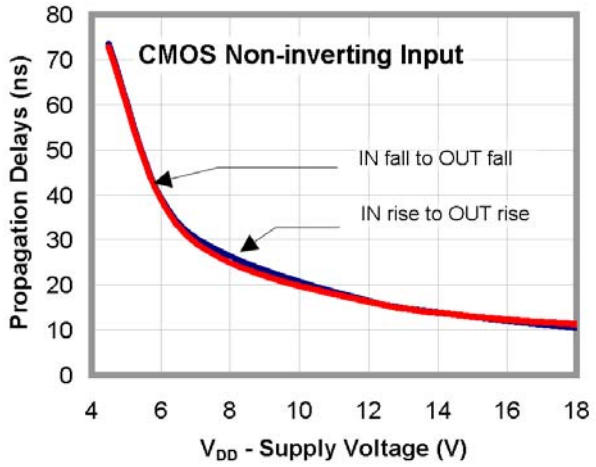


**Figure 31. Propagation Delay vs. Supply Voltage**

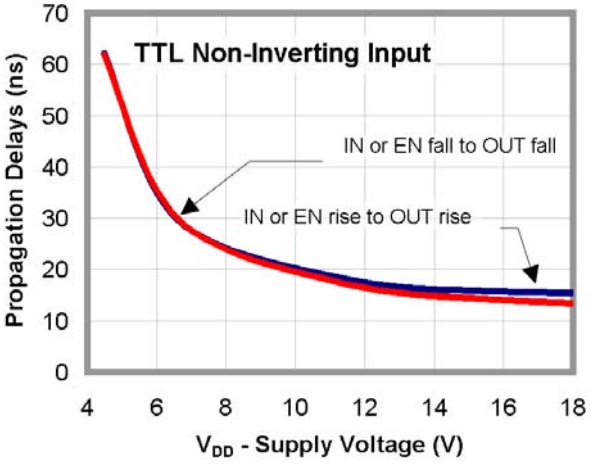


**Figure 32. Propagation Delay vs. Supply Voltage**

## Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}$=12 V unless otherwise noted.

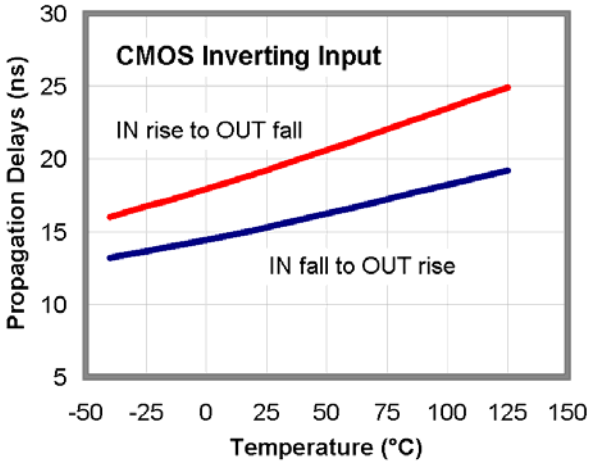


Figure 33. Propagation Delays vs. Temperature

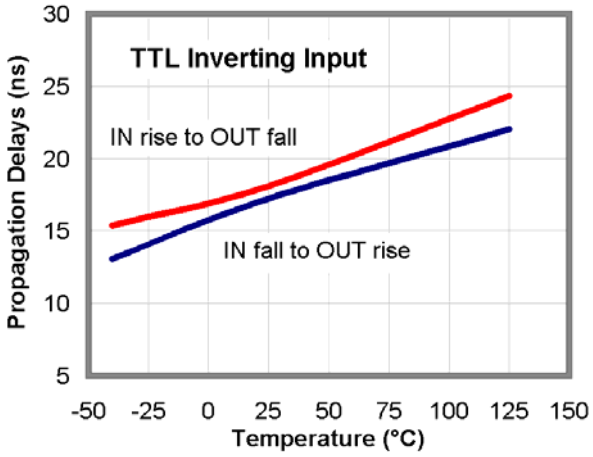


Figure 34. Propagation Delays vs. Temperature

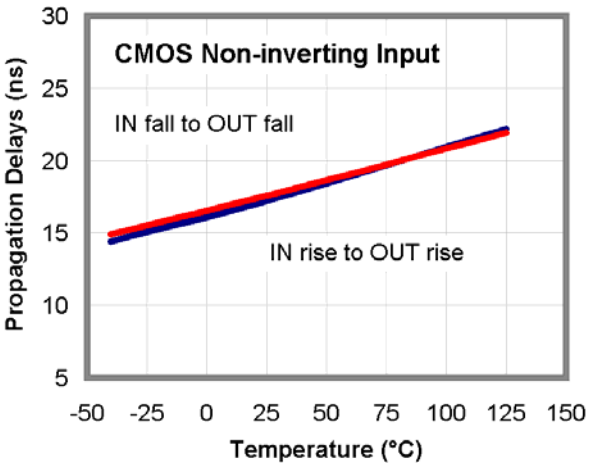


Figure 35. Propagation Delays vs. Temperature

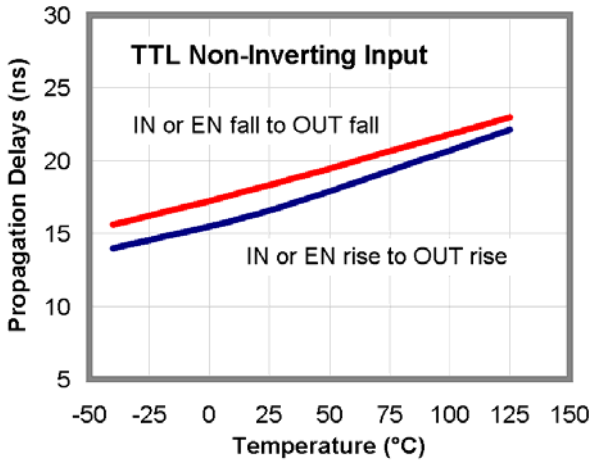


Figure 36. Propagation Delays vs. Temperature

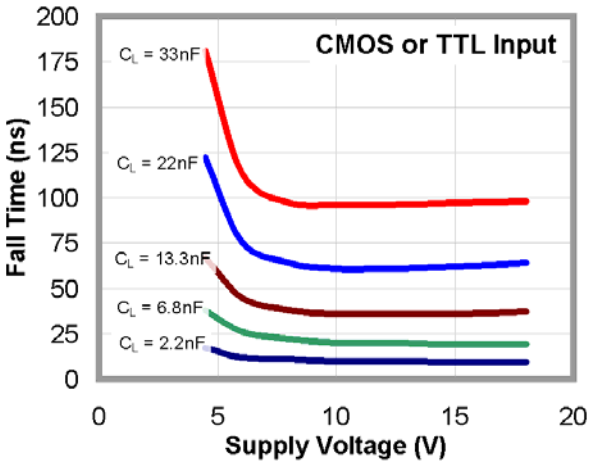


Figure 37. Fall Time vs. Supply Voltage

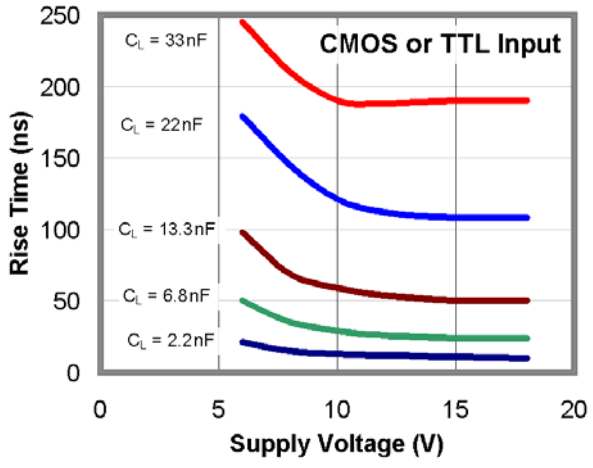


Figure 38. Rise Time vs. Supply Voltage

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## Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}$=12 V unless otherwise noted.

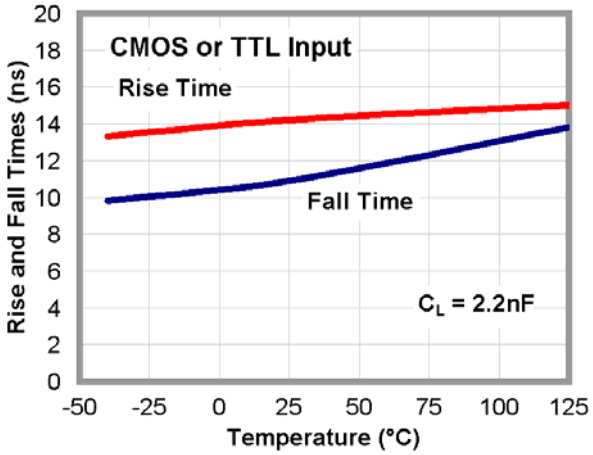


**Figure 39. Rise and Fall Times vs. Temperature**

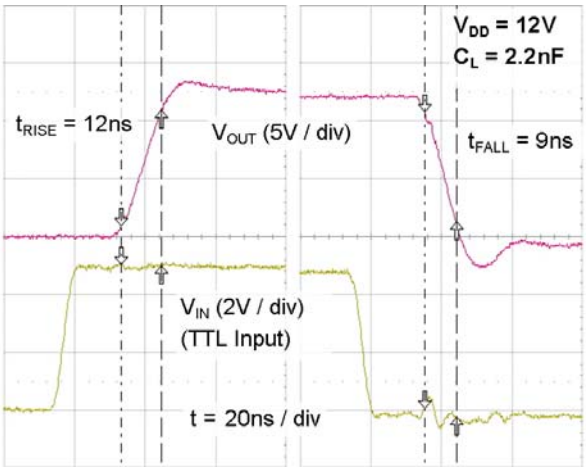


**Figure 40. Rise/Fall Waveforms with 2.2 nF Load**

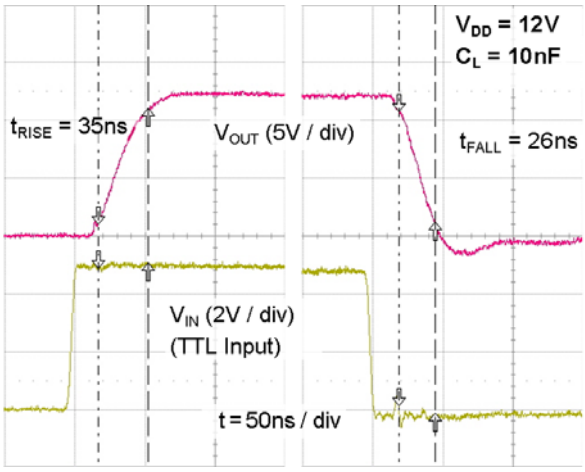


**Figure 41. Rise/Fall Waveforms with 10 nF Load**

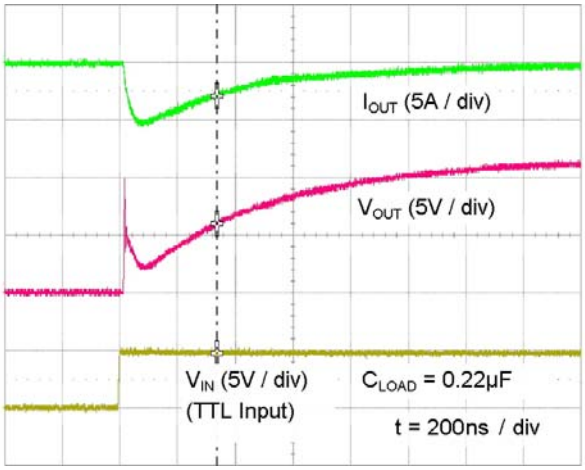


**Figure 42. Quasi-Static Source Current with $V_{DD}$=12 V[16]**

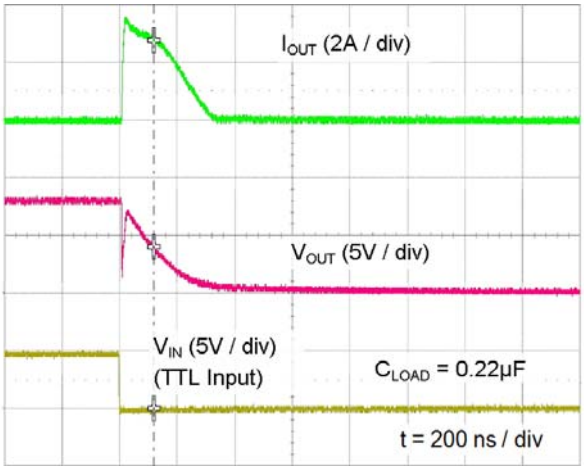


**Figure 43. Quasi-Static Sink Current with $V_{DD}$=12 V[16]**

## Typical Performance Characteristics

Typical characteristics are provided at 25°C and $V_{DD}$=12 V unless otherwise noted.

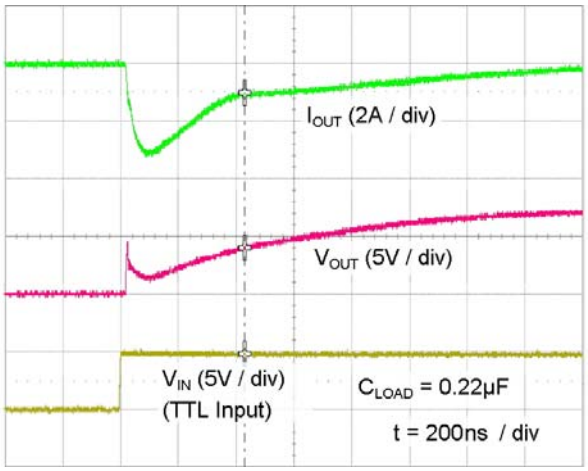


**Figure 44. Quasi-Static Source Current with $V_{DD}$=8 V(16)**

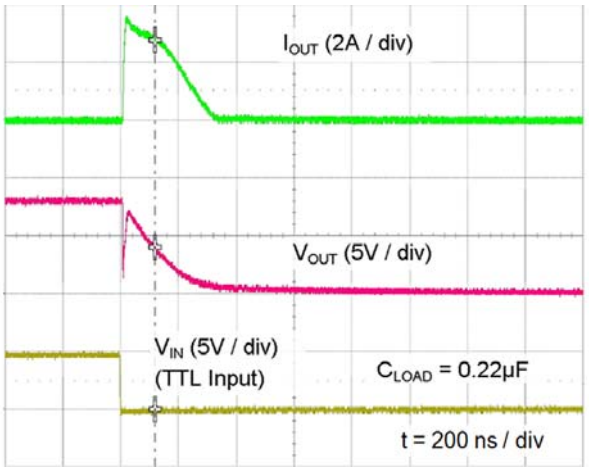


**Figure 45. Quasi-Static Sink Current with $V_{DD}$=8 V(16)**

**Notes:**

15. For any inverting inputs pulled low, non-inverting inputs pulled high, or outputs driven high, static $I_{DD}$ increases by the current flowing through the corresponding pull-up/down resistor shown in the block diagram.
16. The initial spike in each current waveform is a measurement artifact caused by the stray inductance of the current-measurement loop.

## Test Circuit

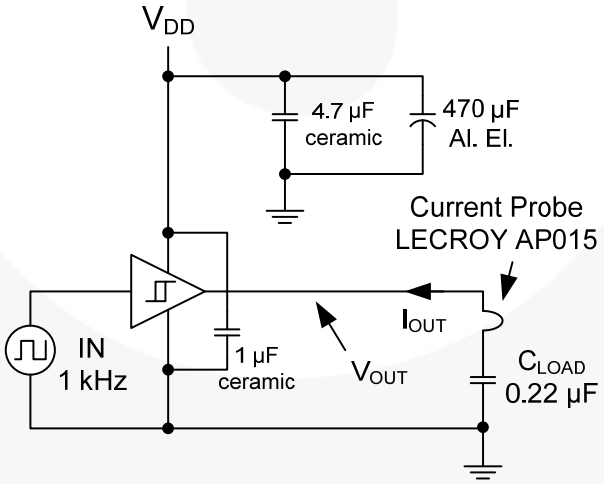


**Figure 46. Quasi-Static $I_{OUT}$ / $V_{OUT}$ Test Circuit**

# Applications Information

## Input Thresholds

Each member of the FAN322x driver family consists of two identical channels that may be used independently at rated current or connected in parallel to double the individual current capacity. In the FAN3223 and FAN3224, channels A and B can be enabled or disabled independently using ENA or ENB, respectively. The EN pin has TTL thresholds for parts with either CMOS or TTL input thresholds. If ENA and ENB are not connected, an internal pull-up resistor enables the driver channels by default. ENA and ENB have TTL thresholds in parts with either TTL or CMOS INx threshold. If the channel A and channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB should be connected and driven together.

The FAN322x family offers versions in either TTL or CMOS input thresholds. In the FAN322xT, the input thresholds meet industry-standard TTL-logic thresholds independent of the $V_{DD}$ voltage, and there is a hysteresis voltage of approximately 0.4 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/µs or faster, so a rise time from 0 to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation.

In the FAN322xC, the logic input thresholds are dependent on the $V_{DD}$ level and, with $V_{DD}$ of 12V, the logic rising edge threshold is approximately 55% of $V_{DD}$ and the input falling edge threshold is approximately 38% of $V_{DD}$. The CMOS input configuration offers a hysteresis voltage of approximately 17% of $V_{DD}$. The CMOS inputs can be used with relatively slow edges (approaching DC) if good decoupling and bypass techniques are incorporated in the system design to prevent noise from violating the input voltage hysteresis window. This allows setting precise timing intervals by fitting an R-C circuit between the controlling signal and the IN pin of the driver. The slow rising edge at the IN pin of the driver introduces a delay between the controlling signal and the OUT pin of the driver.

## Static Supply Current

In the $I_{DD}$ (static) typical performance characteristics *(Figure 12 - Figure 14 and Figure 19 - Figure 21)*, the curve is produced with all inputs/enables floating (OUT is low) and indicates the lowest static $I_{DD}$ current for the tested configuration. For other states, additional current flows through the 100 kΩ resistors on the inputs and outputs shown in the block diagram of each part *(see Figure 5 - Figure 7)*. In these cases, the actual static $I_{DD}$ current is the value obtained from the curves plus this additional current.

## MillerDrive™ Gate Drive Technology

FAN322x gate drivers incorporate the MillerDrive™ architecture shown in Figure 47. For the output stage, a combination of bipolar and MOS devices provide large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 $V_{DD}$ and the MOS devices pull the output to the HIGH or LOW rail.

The purpose of the MillerDrive™ architecture is to speed up switching by providing high current during the Miller plateau region when the gate-drain capacitance of the MOSFET is being charged or discharged as part of the turn-on / turn-off process.

For applications that have zero voltage switching during the MOSFET turn-on or turn-off interval, the driver supplies high peak current for fast switching even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched ON.

The output pin slew rate is determined by $V_{DD}$ voltage and the load on the output. It is not user adjustable, but a series resistor can be added if a slower rise or fall time at the MOSFET gate is needed.

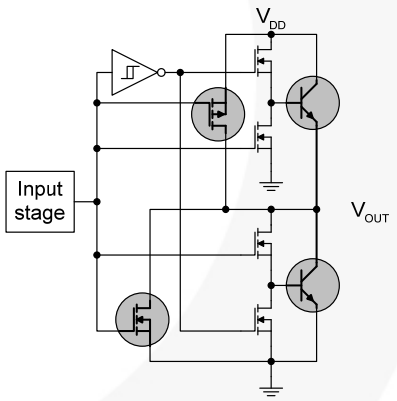


**Figure 47. MillerDrive™ Output Architecture**

## Under-Voltage Lockout

The FAN322x startup logic is optimized to drive ground-referenced N-channel MOSFETs with an under-voltage lockout (UVLO) function to ensure that the IC starts up in an orderly fashion. When $V_{DD}$ is rising, yet below the 3.9 V operational level, this circuit holds the output LOW, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.2 V before the part shuts down. This hysteresis helps prevent chatter when low $V_{DD}$ supply voltages have noise from the power switching. This configuration is not suitable for driving high-side P-channel MOSFETs because the low output voltage of the driver would turn the P-channel MOSFET ON with $V_{DD}$ below 3.9 V.

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## $V_{DD}$ Bypass Capacitor Guidelines

To enable this IC to turn a device ON quickly, a local high-frequency bypass capacitor, $C_{BYP}$, with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to the bulk electrolytic capacitance of 10 µF to 47 µF commonly found on the driver and controller bias circuits.

A typical criterion for choosing the value of $C_{BYP}$ is to keep the ripple voltage on the $V_{DD}$ supply to ≤5%. This is often achieved with a value ≥20 times the equivalent load capacitance $C_{EQV}$, defined here as $Q_{GATE}/V_{DD}$. Ceramic capacitors of 0.1 µF to 1 µF or larger are common choices, as are dielectrics, such as X5R and X7R with good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of $C_{BYP}$ may be increased to 50-100 times the $C_{EQV}$, or $C_{BYP}$ may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1-10 nF mounted closest to the VDD and GND pins to carry the higher frequency components of the current pulses. The bypass capacitor must provide the pulsed current from both of the driver channels and, if the drivers are switching simultaneously, the combined peak current sourced from the $C_{BYP}$ would be twice as large as when a single channel is switching.

## Layout and Connection Guidelines

The FAN3223-25 family of gate drivers incorporates fast-reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 4 A to facilitate voltage transition times from under 10 ns to over 150 ns. The following layout and connection guidelines are strongly recommended:

- Keep high-current output and power ground paths separate logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds at driver inputs and enable pins.
- Keep the driver as close to the load as possible to minimize the length of high-current traces. This reduces the series inductance to improve high-speed switching, while reducing the loop area that can radiate EMI to the driver inputs and surrounding circuitry.
- If the inputs to a channel are not externally connected, the internal 100 kΩ resistors indicated on block diagrams command a low output. In noisy environments, it may be necessary to tie inputs of an unused channel to VDD or GND using short traces to prevent noise from causing spurious output switching.
- Many high-speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be obvious if the circuit is tested in breadboard or non-optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The FAN322x is compatible with many other industry-standard drivers. In single input parts with enable pins, there is an internal 100 kΩ resistor tied to VDD to enable the driver by default; this should be considered in the PCB layout.
- The turn-on and turn-off current paths should be minimized, as discussed in the following section.

Figure 48 shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET ON. The current is supplied from the local bypass capacitor, $C_{BYP}$, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized $C_{BYP}$ acts to contain the high peak current pulses within this driver-MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

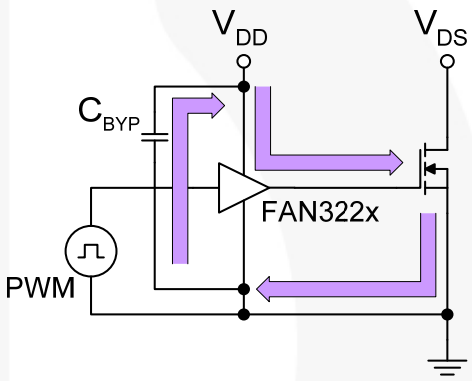


**Figure 48. Current Path for MOSFET Turn-On**

Figure 49 shows the current path when the gate driver turns the MOSFET OFF. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn-off times, the resistance and inductance in this path should be minimized.

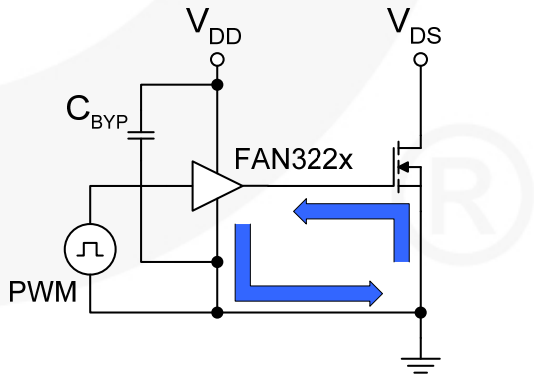


**Figure 49. Current Path for MOSFET Turn-Off**

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## Truth Table of Logic Operation

The FAN3225 truth table indicates the operational states using the dual-input configuration. In a non-inverting driver configuration, the IN- pin should be a logic LOW signal. If the IN- pin is connected to logic HIGH, a disable function is realized, and the driver output remains LOW regardless of the state of the IN+ pin.

| IN+ | IN- | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

In the non-inverting driver configuration in Figure 50, the IN- pin is tied to ground and the input signal (PWM) is applied to IN+ pin. The IN- pin can be connected to logic HIGH to disable the driver and the output remains LOW, regardless of the state of the IN+ pin.

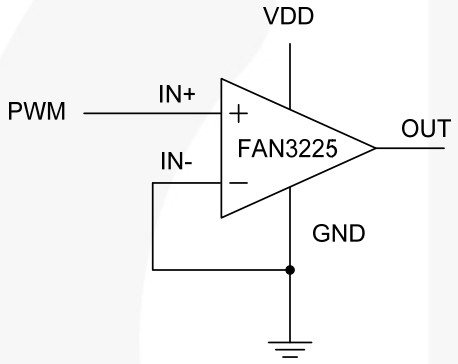


**Figure 50. Dual-Input Driver Enabled, Non-Inverting Configuration**

In the inverting driver application in Figure 51, the IN+ pin is tied HIGH. Pulling the IN+ pin to GND forces the output LOW, regardless of the state of the IN- pin.

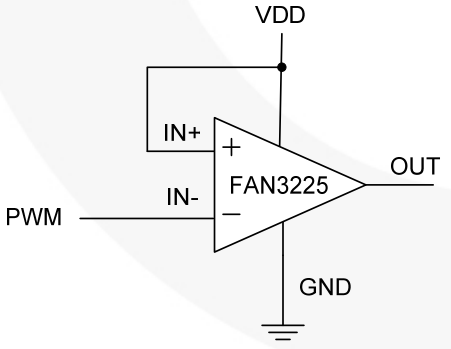


**Figure 51. Dual-Input Driver Enabled, Inverting Configuration**

## Operational Waveforms

At power-up, the driver output remains LOW until the $V_{DD}$ voltage reaches the turn-on threshold. The magnitude of the OUT pulses rises with $V_{DD}$ until steady-state $V_{DD}$ is reached. The non-inverting operation illustrated in Figure 52 shows that the output remains LOW until the UVLO threshold is reached, then the output is in-phase with the input.

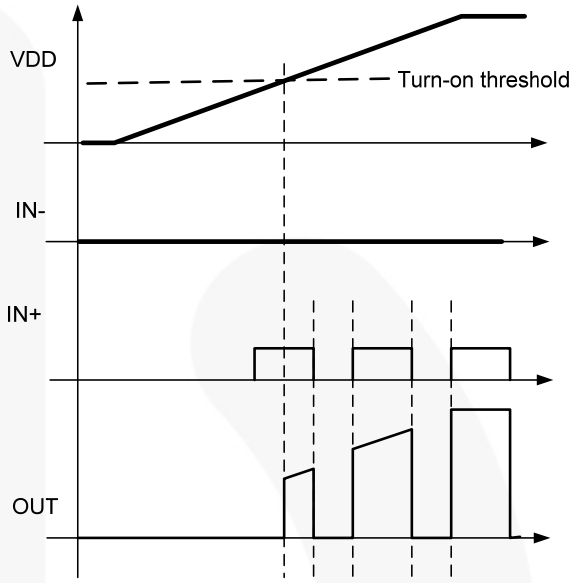


**Figure 52. Non-Inverting Startup Waveforms**

For the inverting configuration of Figure 51, startup waveforms are shown in Figure 53. With IN+ tied to VDD and the input signal applied to IN–, the OUT pulses are inverted with respect to the input. At power-up, the inverted output remains LOW until the $V_{DD}$ voltage reaches the turn-on threshold, then it follows the input with inverted phase.

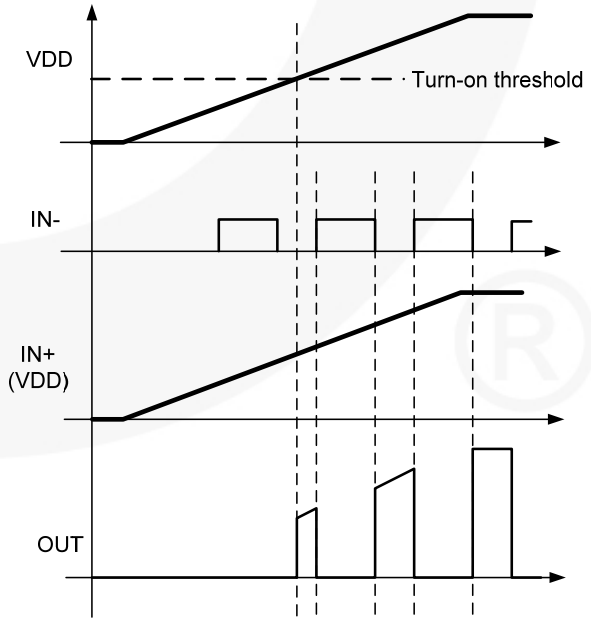


**Figure 53. Inverting Startup Waveforms**

## Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, $P_{GATE}$ and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \quad (1)$$

$P_{GATE}$ (Gate Driving Loss): The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate-source voltage, $V_{GS}$, with gate charge, $Q_G$, at switching frequency, $f_{SW}$, is determined by:

$$P_{GATE} = Q_G \bullet V_{GS} \bullet f_{SW} \bullet n \quad (2)$$

where n is the number of driver channels in use (1 or 2).

$P_{DYNAMIC}$ (Dynamic Pre-Drive / Shoot-through Current): A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistors. The internal current consumption ($I_{DYNAMIC}$) can be estimated using the graphs in Figure 15 and Figure 16 of the Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from $V_{DD}$ under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \bullet V_{DD} \bullet n \quad (3)$$

where n is the number of driver ICs in use. Note that n is usually be one IC even if the IC has two channels, unless two or more.driver ICs are in parallel to drive a large load.

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming $\Psi_{JB}$ was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \bullet \Psi_{JB} + T_B \quad (4)$$

where:

$T_J$ = driver junction temperature;

$\Psi_{JB}$ = (psi) thermal characterization parameter relating temperature rise to total power dissipation; and

$T_B$ = board temperature in location as defined in the Thermal Characteristics table.

To give a numerical example, assume for a 12 V $V_{DD}$ ($V_{BIAS}$) system, the synchronous rectifier switches of Figure 54 have a total gate charge of 60 nC at $V_{GS}$ = 7 V. Therefore, two devices in parallel would have 120 nC gate charge. At a switching frequency of 300 kHz, the total power dissipation is:

$$P_{GATE} = 120\ nC \bullet 7\ V \bullet 300\ kHz \bullet 2 = 0.504\ W \quad (5)$$

$$P_{DYNAMIC} = 3.0\ mA \bullet 12\ V \bullet 1 = 0.036\ W \quad (6)$$

$$P_{TOTAL} = 0.540\ W \quad (7)$$

The SOIC-8 has a junction-to-board thermal characterization parameter of $\Psi_{JB}$ = 42°C/W. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150°C; with 80% derating, $T_J$ would be limited to 120°C. Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120°C:

$$T_{B,MAX} = T_J - P_{TOTAL} \bullet \Psi_{JB} \quad (8)$$

$$T_{B,MAX} = 120°C - 0.54\ W \bullet 42°C/W = 97°C \quad (9)$$

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## Typical Application Diagrams

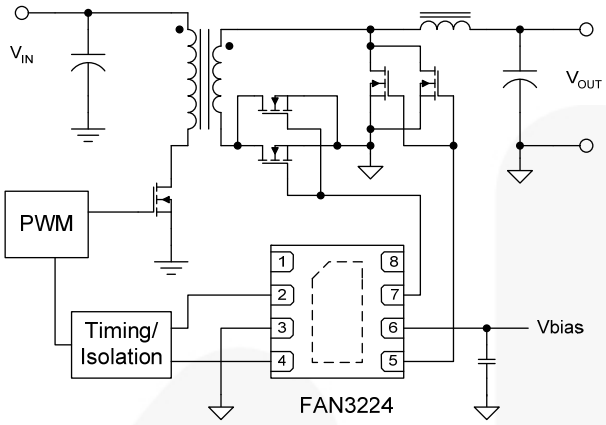


**Figure 54. High Current Forward Converter with Synchronous Rectification**

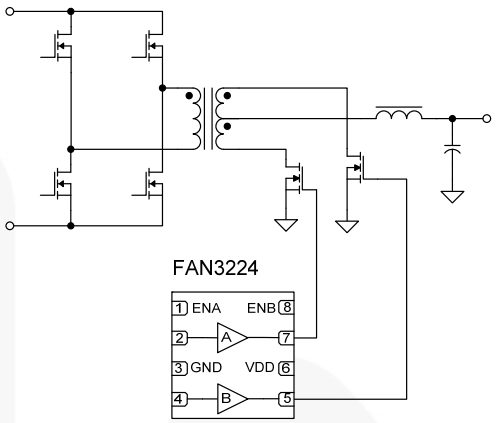


**Figure 55. Center-Tapped Bridge Output with Synchronous Rectifiers**

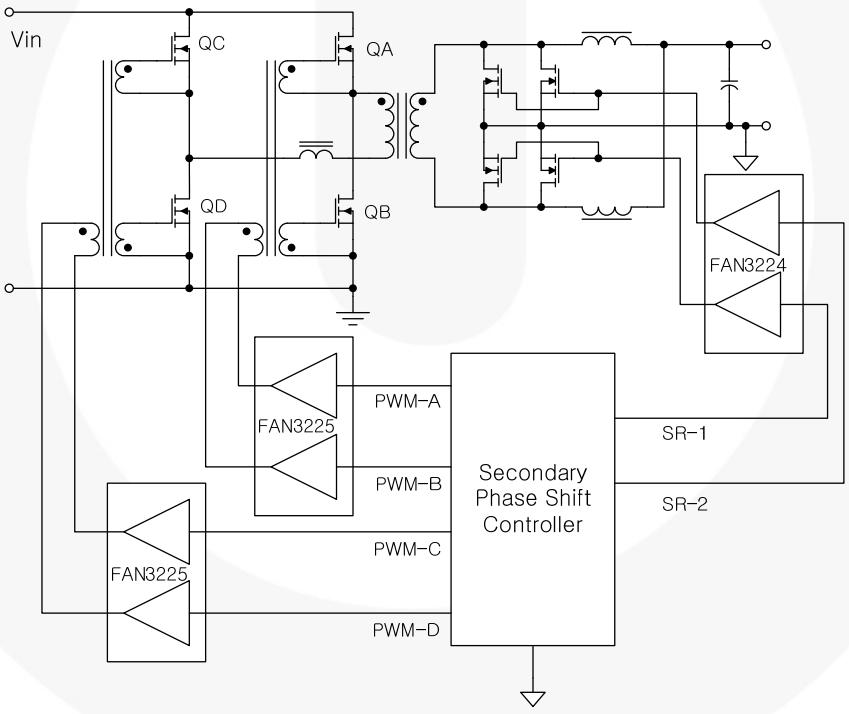


**Figure 56. Secondary Controlled Full Bridge with Current Doubler Output, Synchronous Rectifiers (Simplified)**

**Table 1. Related Products**

| Type | Part Number | Gate Drive[17] (Sink/Src) | Input Threshold | Logic | Package |
|---|---|---|---|---|---|
| Single 1 A | FAN3111C | +1.1 A / -0.9 A | CMOS | Single Channel of Dual-Input/Single-Output | SOT23-5, MLP6 |
| Single 1 A | FAN3111E | +1.1 A / -0.9 A | External[18] | Single Non-Inverting Channel with External Reference | SOT23-5, MLP6 |
| Single 2 A | FAN3100C | +2.5 A / -1.8 A | CMOS | Single Channel of Two-Input/One-Output | SOT23-5, MLP6 |
| Single 2 A | FAN3100T | +2.5 A / -1.8 A | TTL | Single Channel of Two-Input/One-Output | SOT23-5, MLP6 |
| Single 2 A | FAN3180 | +2.4 A / -1.6 A | TTL | Single Non-Inverting Channel + 3.3-V LDO | SOT23-5 |
| Dual 2 A | FAN3216T | +2.4 A / -1.6 A | TTL | Dual Inverting Channels | SOIC8 |
| Dual 2 A | FAN3217T | +2.4 A / -1.6 A | TTL | Dual Non-Inverting Channels | SOIC8 |
| Dual 2 A | FAN3226C | +2.4 A / -1.6 A | CMOS | Dual Inverting Channels + Dual Enable | SOIC8, MLP8 |
| Dual 2 A | FAN3226T | +2.4 A / -1.6 A | TTL | Dual Inverting Channels + Dual Enable | SOIC8, MLP8 |
| Dual 2 A | FAN3227C | +2.4 A / -1.6 A | CMOS | Dual Non-Inverting Channels + Dual Enable | SOIC8, MLP8 |
| Dual 2 A | FAN3227T | +2.4 A / -1.6 A | TTL | Dual Non-Inverting Channels + Dual Enable | SOIC8, MLP8 |
| Dual 2 A | FAN3228C | +2.4 A / -1.6 A | CMOS | Dual Channels of Two-Input/One-Output, Pin Config.1 | SOIC8, MLP8 |
| Dual 2 A | FAN3228T | +2.4 A / -1.6 A | TTL | Dual Channels of Two-Input/One-Output, Pin Config.1 | SOIC8, MLP8 |
| Dual 2 A | FAN3229C | +2.4 A / -1.6 A | CMOS | Dual Channels of Two-Input/One-Output, Pin Config.2 | SOIC8, MLP8 |
| Dual 2 A | FAN3229T | +2.4 A / -1.6 A | TTL | Dual Channels of Two-Input/One-Output, Pin Config.2 | SOIC8, MLP8 |
| Dual 2 A | FAN3268T | +2.4 A / -1.6 A | TTL | 20 V Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables | SOIC8 |
| Dual 2 A | FAN3278T | +2.4 A / -1.6 A | TTL | 30 V Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables | SOIC8 |
| Dual 4 A | FAN3213T | +4.3 A / -2.8 A | TTL | Dual Inverting Channels | SOIC8 |
| Dual 4 A | FAN3214T | +4.3 A / -2.8 A | TTL | Dual Non-Inverting Channels | SOIC8 |
| **Dual 4 A** | **FAN3223C** | **+4.3 A / -2.8 A** | **CMOS** | **Dual Inverting Channels + Dual Enable** | **SOIC8, MLP8** |
| **Dual 4 A** | **FAN3223T** | **+4.3 A / -2.8 A** | **TTL** | **Dual Inverting Channels + Dual Enable** | **SOIC8, MLP8** |
| **Dual 4 A** | **FAN3224C** | **+4.3 A / -2.8 A** | **CMOS** | **Dual Non-Inverting Channels + Dual Enable** | **SOIC8, MLP8** |
| **Dual 4 A** | **FAN3224T** | **+4.3 A / -2.8 A** | **TTL** | **Dual Non-Inverting Channels + Dual Enable** | **SOIC8, MLP8** |
| **Dual 4 A** | **FAN3225C** | **+4.3 A / -2.8 A** | **CMOS** | **Dual Channels of Two-Input/One-Output** | **SOIC8, MLP8** |
| **Dual 4 A** | **FAN3225T** | **+4.3 A / -2.8 A** | **TTL** | **Dual Channels of Two-Input/One-Output** | **SOIC8, MLP8** |
| Single 9 A | FAN3121C | +9.7 A / -7.1 A | CMOS | Single Inverting Channel + Enable | SOIC8, MLP8 |
| Single 9 A | FAN3121T | +9.7 A / -7.1 A | TTL | Single Inverting Channel + Enable | SOIC8, MLP8 |
| Single 9 A | FAN3122T | +9.7 A / -7.1 A | CMOS | Single Non-Inverting Channel + Enable | SOIC8, MLP8 |
| Single 9 A | FAN3122C | +9.7 A / -7.1 A | TTL | Single Non-Inverting Channel + Enable | SOIC8, MLP8 |
| Dual 12 A | FAN3240 | +12.0 A | TTL | Dual-Coil Relay Driver, Timing Config. 0 | SOIC8 |
| Dual 12 A | FAN3241 | +12.0 A | TTL | Dual-Coil Relay Driver, Timing Config. 1 | SOIC8 |

**Notes:**

17. Typical currents with OUTx at 6 V and $V_{DD}$=12 V.
18. Thresholds proportional to an externally supplied reference voltage.

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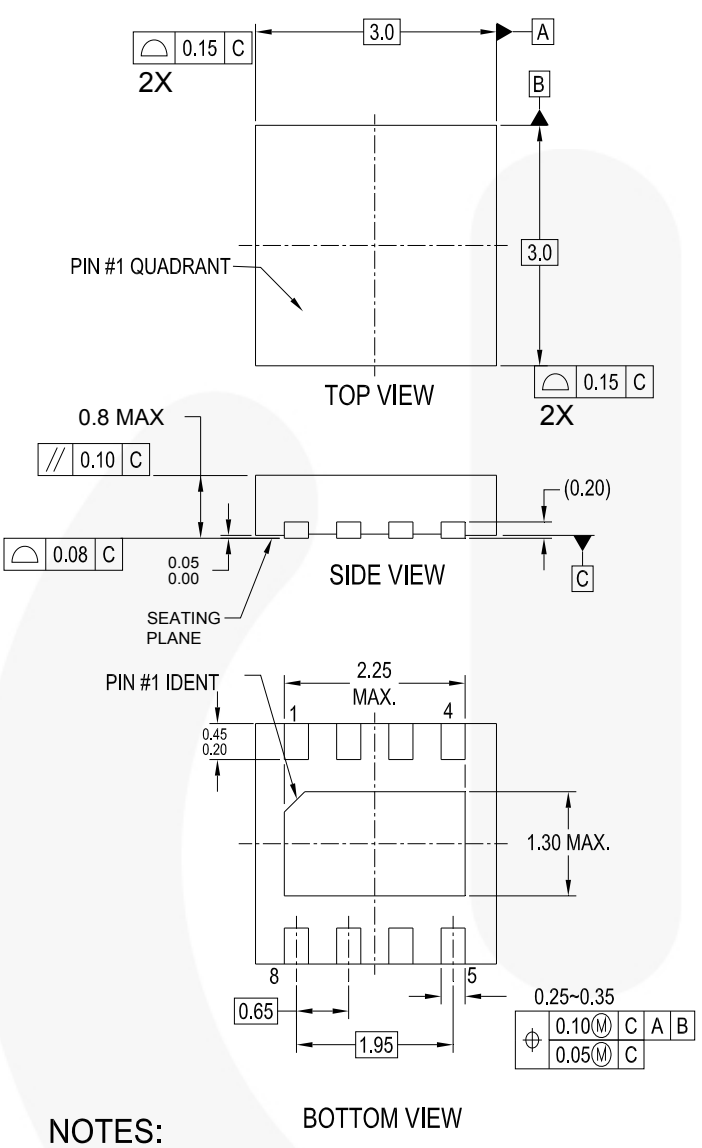


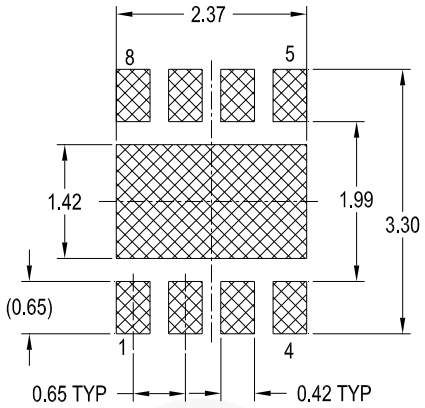


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NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VEEC, DATED 11/2001

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. FILENAME: MKT-MLP08Drev2

**Figure 57. 3x3 mm, 8-Lead Molded Leadless Package (MLP)**

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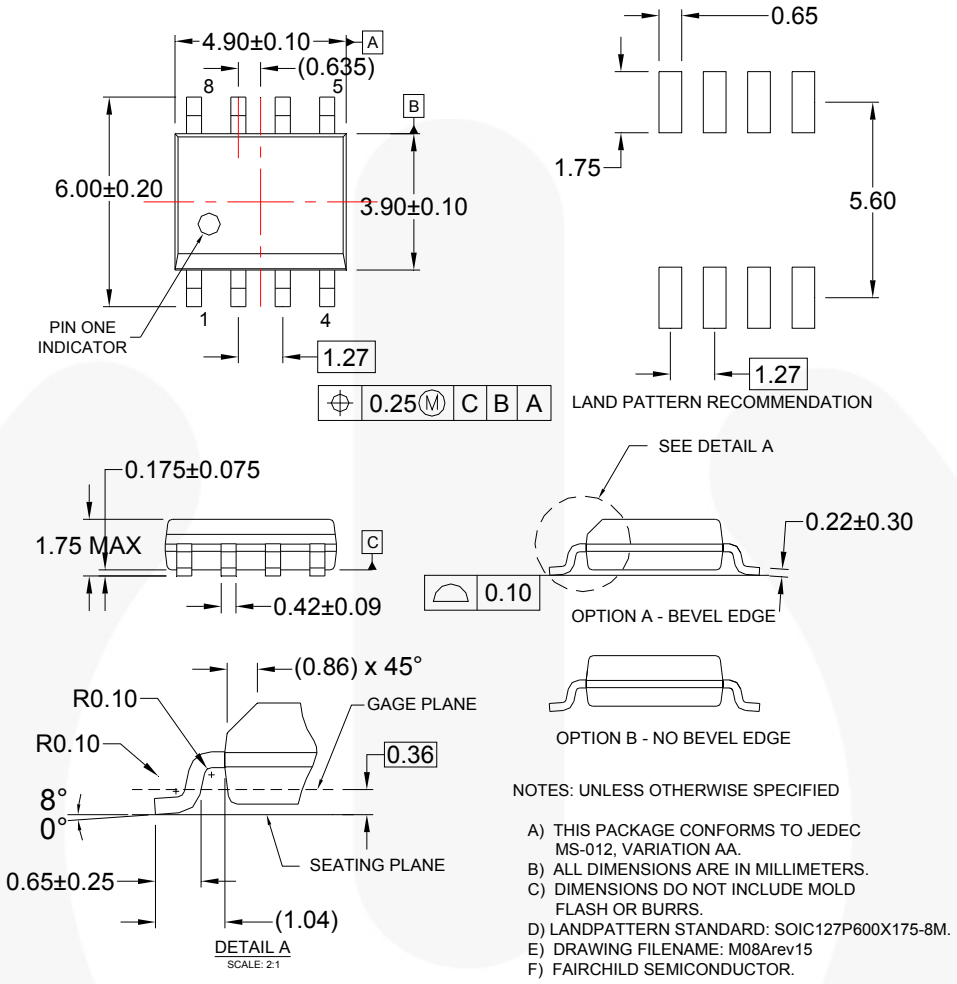


**Figure 58. 8-Lead Small Outline Integrated Circuit (SOIC)**

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