

J309, J310

Preferred Device

JFET VHF/UHF Amplifiers

N-Channel — Depletion

Features

- Pb-Free Packages are Available*

MAXIMUM RATINGS

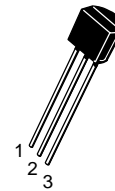
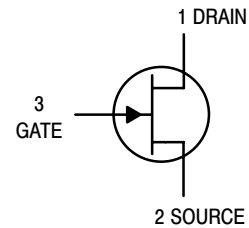
| Rating | Symbol | Value | Unit |
|--|-----------|-------------|-------------|
| Drain-Source Voltage | V_{DS} | 25 | Vdc |
| Gate-Source Voltage | V_{GS} | 25 | Vdc |
| Forward Gate Current | I_{GF} | 10 | mAdc |
| Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above = 25°C | P_D | 350 2.8 | mW mW/°C |
| Junction Temperature Range | T_J | -65 to +125 | °C |
| Storage Temperature Range | T_{stg} | -65 to +150 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



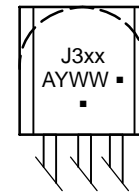
ON Semiconductor®

<http://onsemi.com>



TO-92
CASE 29-11
STYLE 5

MARKING DIAGRAM



J3xx = Device Code
xx = 09 or 10
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

J309, J310

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------------------|---------------|----------------|----------------|--------------|
| OFF CHARACTERISTICS | | | | | |
| Gate–Source Breakdown Voltage (I _G = –1.0 μAdc, V _{DS} = 0) | V _{(BR)GSS} | –25 | – | – | Vdc |
| Gate Reverse Current (V _{GS} = –15 Vdc, V _{DS} = 0, T _A = 25°C) (V _{GS} = –15 Vdc, V _{DS} = 0, T _A = +125°C) | I _{GSS} | – | – | –1.0 –1.0 | nAdc μAdc |
| Gate Source Cutoff Voltage (V _{DS} = 10 Vdc, I _D = 1.0 nAdc) | V _{GS(off)} | –1.0 –2.0 | – | –4.0 –6.5 | Vdc |
| ON CHARACTERISTICS | | | | | |
| Zero–Gate–Voltage Drain Current ⁽¹⁾ (V _{DS} = 10 Vdc, V _{GS} = 0) | I _{DSS} | 12 24 | – | 30 60 | mAdc |
| Gate–Source Forward Voltage (V _{DS} = 0, I _G = 1.0 mAdc) | V _{GS(f)} | – | – | 1.0 | Vdc |
| SMALL–SIGNAL CHARACTERISTICS | | | | | |
| Common–Source Input Conductance (V _{DS} = 10 Vdc, I _D = 10 mAdc, f = 100 MHz) | Re(y _{is}) | – | 0.7 0.5 | – | mmhos |
| Common–Source Output Conductance (V _{DS} = 10 Vdc, I _D = 10 mAdc, f = 100 MHz) | Re(y _{os}) | – | 0.25 | – | mmhos |
| Common–Gate Power Gain (V _{DS} = 10 Vdc, I _D = 10 mAdc, f = 100 MHz) | G _{pg} | – | 16 | – | dB |
| Common–Source Forward Transconductance (V _{DS} = 10 Vdc, I _D = 10 mAdc, f = 100 MHz) | Re(y _{fs}) | – | 12 | – | mmhos |
| Common–Gate Input Conductance (V _{DS} = 10 Vdc, I _D = 10 mAdc, f = 100 MHz) | Re(y _{ig}) | – | 12 | – | mmhos |
| Common–Source Forward Transconductance (V _{DS} = 10 Vdc, I _D = 10 mAdc, f = 1.0 kHz) | g _{fs} | 10000 8000 | – | 20000 18000 | μmhos |
| Common–Source Output Conductance (V _{DS} = 10 Vdc, I _D = 10 mAdc, f = 1.0 kHz) | g _{os} | – | – | 250 | μmhos |
| Common–Gate Forward Transconductance (V _{DS} = 10 Vdc, I _D = 10 mAdc, f = 1.0 kHz) | g _{fg} | – | 13000 12000 | – | μmhos |
| Common–Gate Output Conductance (V _{DS} = 10 Vdc, I _D = 10 mAdc, f = 1.0 kHz) | g _{og} | – | 100 150 | – | μmhos |
| Gate–Drain Capacitance (V _{DS} = 0, V _{GS} = –10 Vdc, f = 1.0 MHz) | C _{gd} | – | 1.8 | 2.5 | pF |
| Gate–Source Capacitance (V _{DS} = 0, V _{GS} = –10 Vdc, f = 1.0 MHz) | C _{gs} | – | 4.3 | 5.0 | pF |
| FUNCTIONAL CHARACTERISTICS | | | | | |
| Equivalent Short–Circuit Input Noise Voltage (V _{DS} = 10 Vdc, I _D = 10 mAdc, f = 100 Hz) | \bar{e}_n | – | 10 | – | nV/√Hz |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 3.0%.

J309, J310

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------|--------------------|------------------------------|
| J309 | TO-92 | 1000 Units / Bulk |
| J309G | TO-92 (Pb-Free) | |
| J310 | TO-92 | 1000 Units / Bulk |
| J310G | TO-92 (Pb-Free) | |
| J310RLRP | TO-92 | 2000 Units / Tape & Ammo Box |
| J310RLRPG | TO-92 (Pb-Free) | |
| J310ZL1 | TO-92 | 2000 Units / Tape & Ammo Box |
| J310ZL1G | TO-92 (Pb-Free) | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

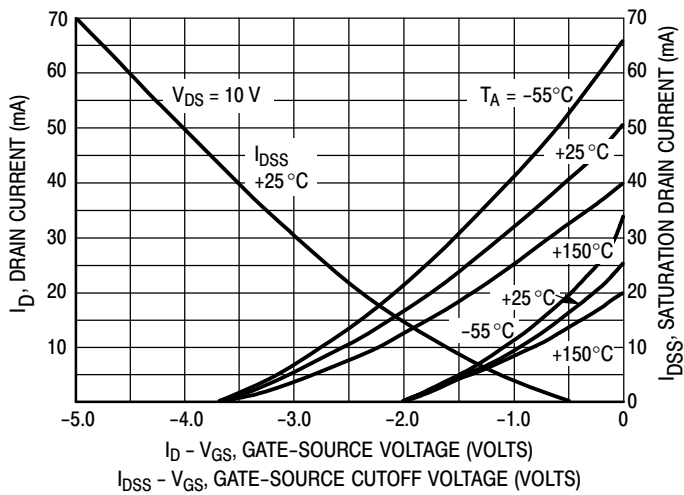


Figure 1. Drain Current and Transfer Characteristics versus Gate-Source Voltage

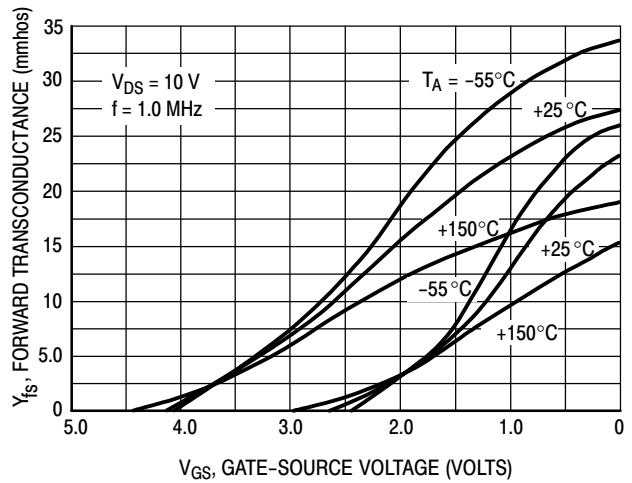


Figure 2. Forward Transconductance versus Gate-Source Voltage

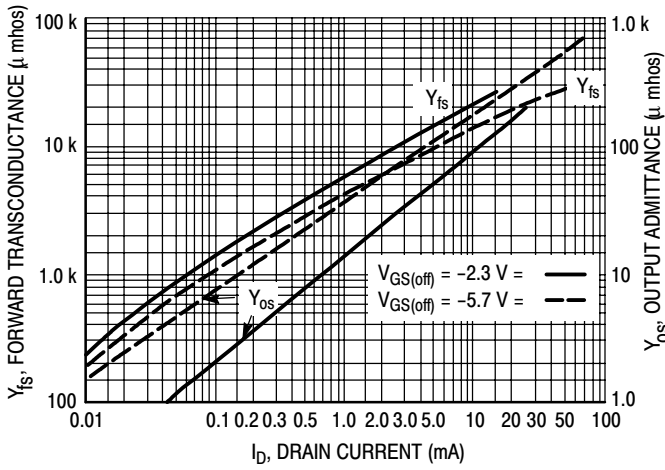


Figure 3. Common-Source Output Admittance and Forward Transconductance versus Drain Current

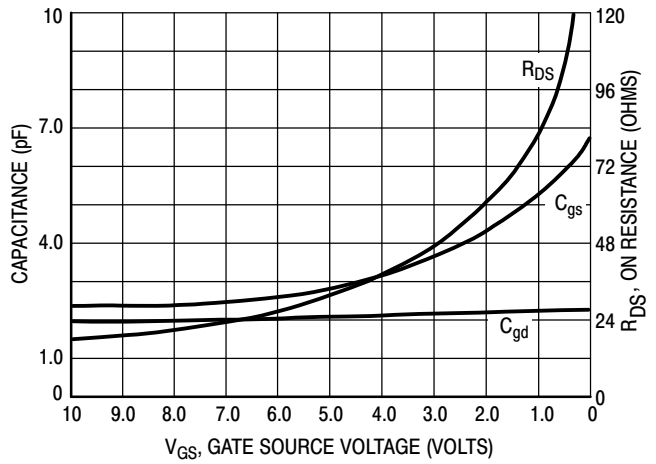


Figure 4. On Resistance and Junction Capacitance versus Gate-Source Voltage

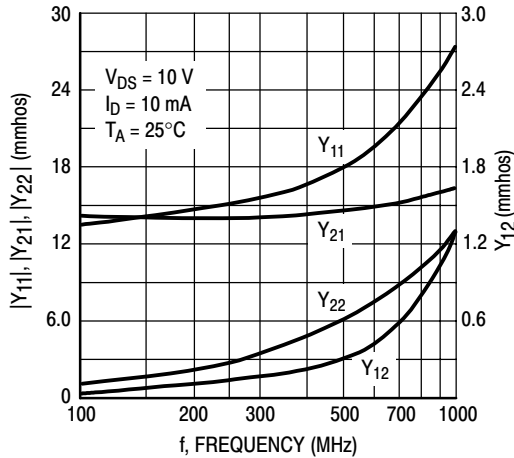


Figure 5. Common-Gate Y Parameter Magnitude versus Frequency

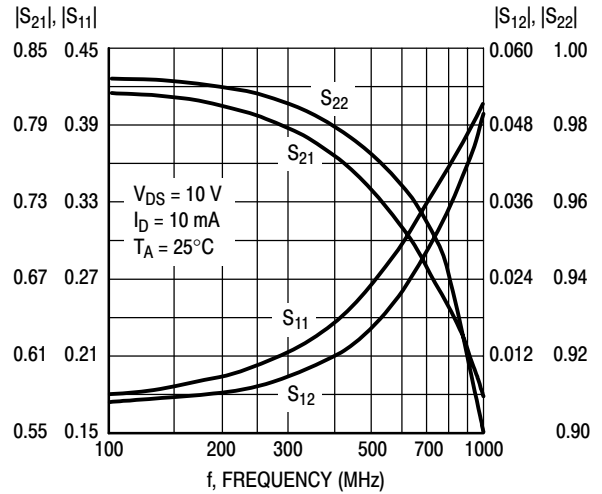


Figure 6. Common-Gate S Parameter Magnitude versus Frequency

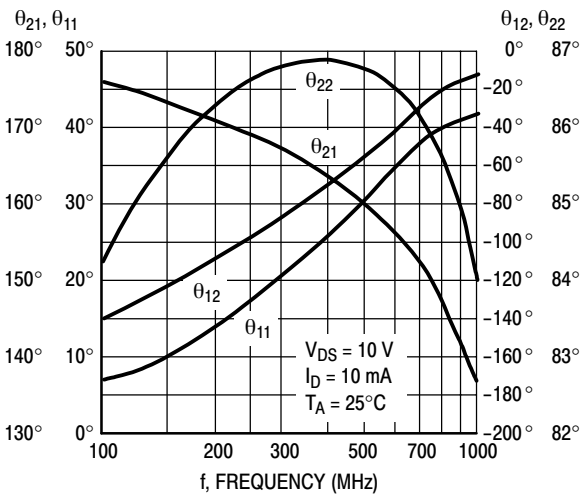


Figure 7. Common-Gate Y Parameter Phase-Angle versus Frequency

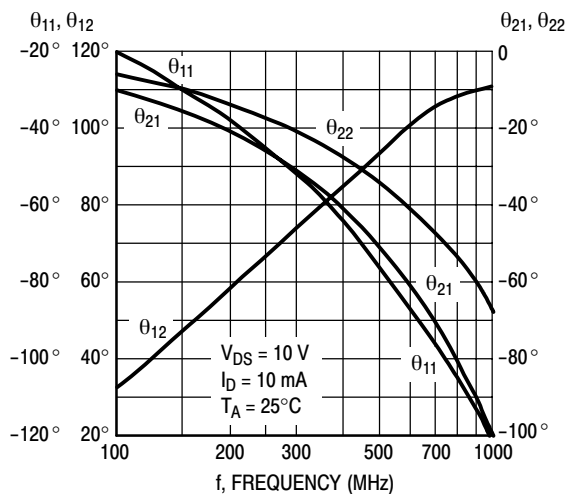
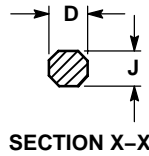
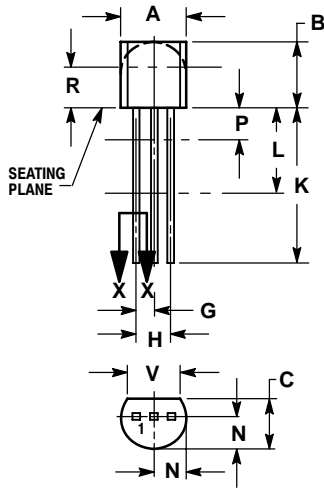


Figure 8. S Parameter Phase-Angle versus Frequency

J309, J310

PACKAGE DIMENSIONS

TO-92 (TO-226) CASE 29-11 ISSUE AL



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.45 | 5.20 |
| B | 0.170 | 0.210 | 4.32 | 5.33 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.016 | 0.021 | 0.407 | 0.533 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.095 | 0.105 | 2.42 | 2.66 |
| J | 0.015 | 0.020 | 0.39 | 0.50 |
| K | 0.500 | --- | 12.70 | --- |
| L | 0.250 | --- | 6.35 | --- |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | --- | 0.100 | --- | 2.54 |
| R | 0.115 | --- | 2.93 | --- |
| V | 0.135 | --- | 3.43 | --- |

STYLE 5:

1. DRAIN
2. SOURCE
3. GATE

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.