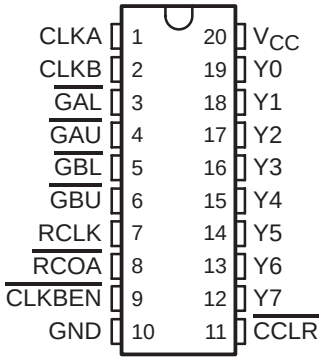
- **Can Be Used as Two 16-Bit Counters or a Single 32-Bit Counter**
- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 25 ns at 5 V (RCLK to Y)**
- **Typical V_{OLP} (Output Ground Bounce) <0.7 V at V_{CC} = 5 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >4.4 V at V_{CC} = 5 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

N OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74LV8154 is a dual 16-bit binary counter with 3-state output registers, designed for 2-V to 5.5-V V_{CC} operation.

This 16-bit counter (A or B) feeds a 16-bit storage register, and each storage register is further divided into an upper byte and lower byte. The $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ inputs are used to select the byte that needs to be output at Y0−Y7. CLKA is the clock for A counter, and CLKB is the clock for B counter. RCLK is the clock for the A and B storage registers. All three clock signals are positive-edge triggered.

A 32-bit counter can be realized by connecting CLKA and CLKB together and by connecting $\overline{RCOA}$ to $\overline{CLKBEN}$.

To ensure the high-impedance state during power up or power down, $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube	SN74LV8154N	SN74LV8154N
	TSSOP − PW	Tube	SN74LV8154PW	LV8154
		Tape and reel	SN74LV8154PWR	

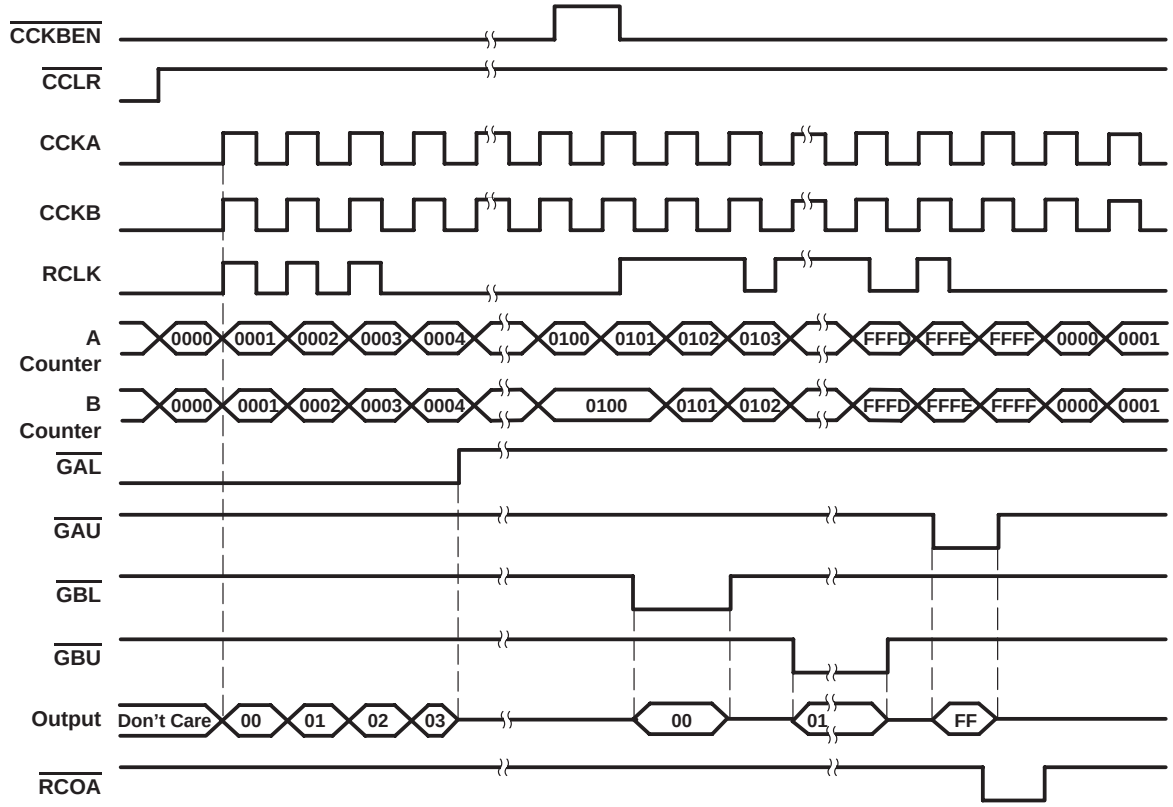
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each buffer)

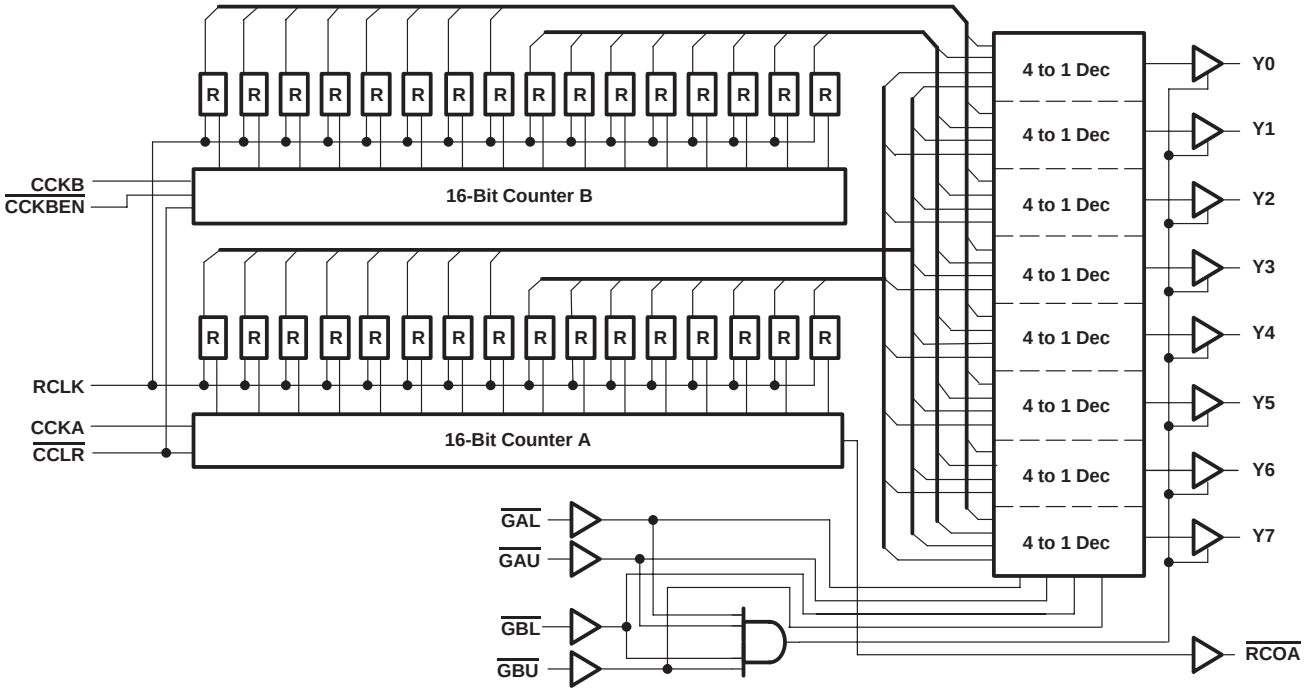
INPUTS				OUTPUT
$\overline{GAL}$	$\overline{GAU}$	$\overline{GBL}$	$\overline{GBU}$	Yn
L	H	H	H	Lower byte in A register
H	L	H	H	Upper byte in A register
H	H	L	H	Lower byte in B register
H	H	H	L	Upper byte in B register
H	H	H	H	Z

Combinations of $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$, other than those shown above, are prohibited. If more than one input is L at the same time, the output data (Y0−Y7) may be invalid.

timing diagram



block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high-impedance
or power-off state, V_O (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −20 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . . ±70 mA
Package thermal impedance, θ_{JA} (see Note 3): N package . . . . . 69°C/W
PW package . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			V_{CC}	MIN	MAX	UNIT
V_{CC}	Supply voltage			2	5.5	V
V_{IH}	High-level input voltage		2 V	1.5		V
			3 V to 3.6 V	$V_{CC} \times 0.7$		
			4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage		2 V		0.5	V
			3 V to 3.6 V		$V_{CC} \times 0.3$	
			4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Input voltage			0	5.5	V
V_O	Output voltage	High or low state		0	V_{CC}	V
		3-state		0	5.5	
I_{OH}	High-level output current	Yn outputs	2 V		−50	µA
			3 V to 3.6 V		−6	mA
			4.5 V to 5.5 V		−12	
		$\overline{RCOA}$	2 V		−50	µA
			3 V to 3.6 V		−6	mA
			4.5 V to 5.5 V		−12	
I_{OL}	Low-level output current	Yn outputs	2 V		50	µA
			3 V to 3.6 V		6	mA
			4.5 V to 5.5 V		12	
		$\overline{RCOA}$	2 V		50	µA
			3 V to 3.6 V		6	mA
			4.5 V to 5.5 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		3 V to 3.6 V		100	ns/V
			4.5 V to 5.5 V		20	
T_A	Operating free-air temperature			−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	Yn	I_{OH} = −50 μA	2 V	1.9			V
		I_{OH} = −6 mA	3 V	2.48			
		I_{OH} = −12 mA	4.5 V	3.8			
	$\overline{RCOA}$	I_{OH} = −50 μA	2 V	1.9			
		I_{OH} = −6 mA	3 V	2.48			
		I_{OH} = −12 mA	4.5 V	3.8			
V_{OL}	Yn	I_{OL} = 50 μA	2 V			0.1	V
		I_{OL} = 6 mA	3 V			0.44	
		I_{OL} = 12 mA	4.5 V			0.55	
	$\overline{RCOA}$	I_{OL} = 50 μA	2 V			0.1	
		I_{OL} = 6 mA	3 V			0.44	
		I_{OL} = 12 mA	4.5 V			0.55	
I_I		V_I = 5.5 V or GND	0 to 5.5 V			±1	μA
I_{OZ}		$V_O = V_{CC}$ or GND	5.5 V			±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			20	μA
I_{off}		V_I or V_O = 0 to 5.5 V	0			5	μA
C_i		$V_I = V_{CC}$ or GND	5 V		3		pF
C_o		$V_O = V_{CC}$ or GND	5 V		5		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
t_w	Pulse duration	CLKA, CLKB, RCLK high or low	10		ns
		$\overline{CCLR}$ low	22		
t_{su}	Setup time	$\overline{CLKBEN}$ low before CLKB↑	13		ns
		$\overline{CCLR}$ high (inactive) before CLKA↑ or CLKB↑	13		
		CLKA↑ or CLKB↑ before RCLK↑	13		
		RCLK↑ before $\overline{GAL}$ or $\overline{GAU}$ or $\overline{GBL}$ or $\overline{GBU}$ low	13		
		$\overline{GAL}$ or $\overline{GAU}$ or $\overline{GBL}$ or $\overline{GBU}$ high (inactive) before RCLK↑	13		
t_h	Hold time	$\overline{CLKBEN}$ low after CLKB↑	0		ns
		CLKA or CLKB after RCLK	0		
t_z†	Z-period	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ all high before one of them switches low	200		ns

† t_z condition: C_L = 50 pF, R_L = 1 kΩ

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
t_w	Pulse duration	CLKA, CLKB, RCLK high or low	10		ns
		$\overline{CCLR}$ low	20		
t_{su}	Setup time	$\overline{CLKBEN}$ low before CLKB↑	10		ns
		$\overline{CCLR}$ high (inactive) before CLKA↑ or CLKB↑	10		
		CLKA↑ or CLKB↑ before RCLK↑	10		
		RCLK↑ before $\overline{GAL}$ or $\overline{GAU}$ or $\overline{GBL}$ or $\overline{GBU}$ low	10		
		$\overline{GAL}$ or $\overline{GAU}$ or $\overline{GBL}$ or $\overline{GBU}$ high (inactive) before RCLK↑	10		
t_h	Hold time	$\overline{CLKBEN}$ low after CLKB↑	0		ns
		CLKA or CLKB after RCLK	0		
t_z†	Z-period	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$ all high before one of them switches low	200		ns

† t_z condition: C_L = 50 pF, R_L = 1 kΩ

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{MAX}			C_L = 15 pF				40		MHz
			C_L = 50 pF				25		
t_{pd}	RCLK	Y	C_L = 15 pF		22		1	38	ns
	CLKA	$\overline{RCOA}$			26		1	44	
t_{PLH}	$\overline{CCLR}$	$\overline{RCOA}$			18		1	32	ns
t_{en}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y			27		1	46	ns
t_{dis}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y			12		1	21	ns
t_{pd}	RCLK	Y	C_L = 50 pF		25		1	42	ns
	CLKA	$\overline{RCOA}$			28		1	46	
t_{PLH}	$\overline{CCLR}$	$\overline{RCOA}$			20		1	35	ns
t_{en}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y			30		1	50	ns
t_{dis}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y			14		1	24	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{MAX}			C_L = 15 pF				40		MHz
			C_L = 50 pF				25		
t_{pd}	RCLK	Y	C_L = 15 pF		14		1	25	ns
	CLKA	$\overline{RCOA}$			16		1	27	
t_{PLH}	$\overline{CCLR}$	$\overline{RCOA}$			12		1	20	ns
t_{en}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y			16		1	28	ns
t_{dis}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y			8		1	15	ns
t_{pd}	RCLK	Y	C_L = 50 pF		16		1	27	ns
	CLKA	$\overline{RCOA}$			17		1	28	
t_{PLH}	$\overline{CCLR}$	$\overline{RCOA}$			13		1	21	ns
t_{en}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y			18		1	30	ns
t_{dis}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y			9		1	16	ns

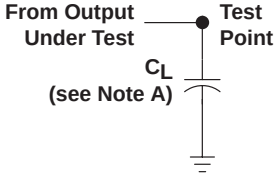
noise characteristics, V_{CC} = 5 V, C_L = 50 pF

PARAMETER		T_A = 25°C			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.7		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.75		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.4		V

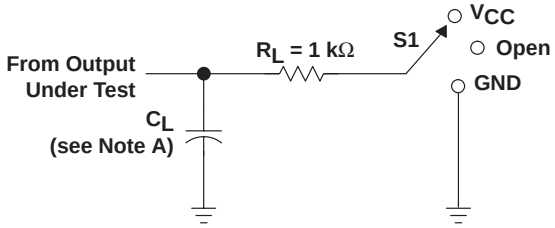
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = No load, CCLK = 10 MHz, RCLK = 1 MHz	56	pF

PARAMETER MEASUREMENT INFORMATION

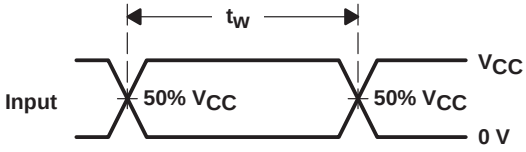


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

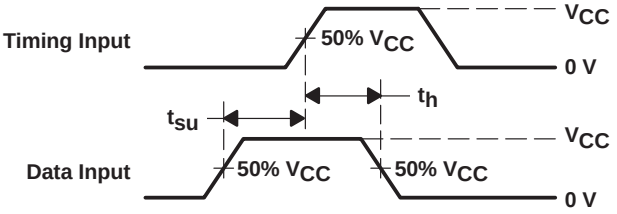


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

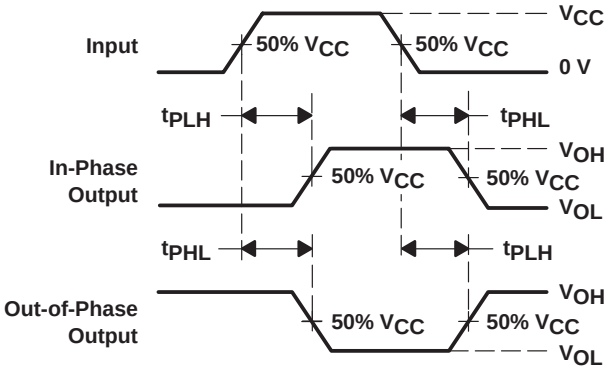
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



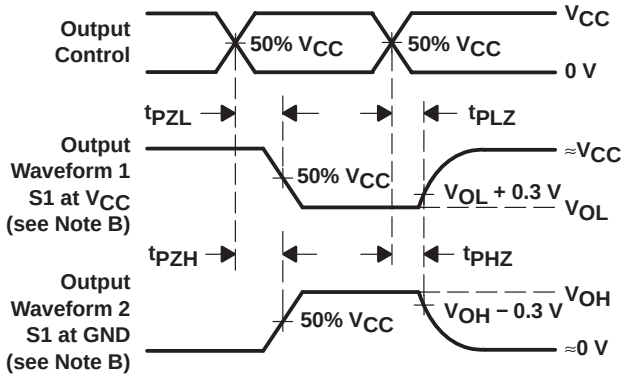
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV8154N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV8154N	Samples
SN74LV8154NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV8154N	Samples
SN74LV8154PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8154	Samples
SN74LV8154PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8154	Samples
SN74LV8154PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV8154	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LV8154 :

- Enhanced Product: SN74LV8154-EP

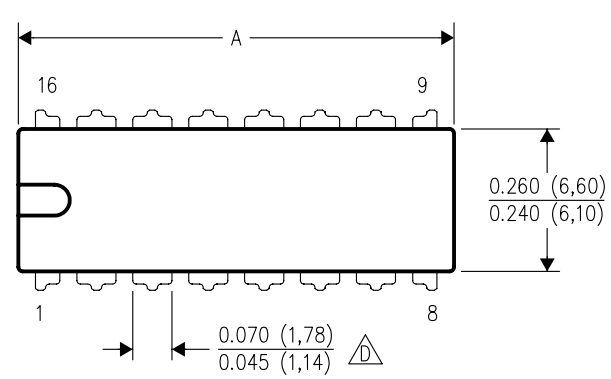
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

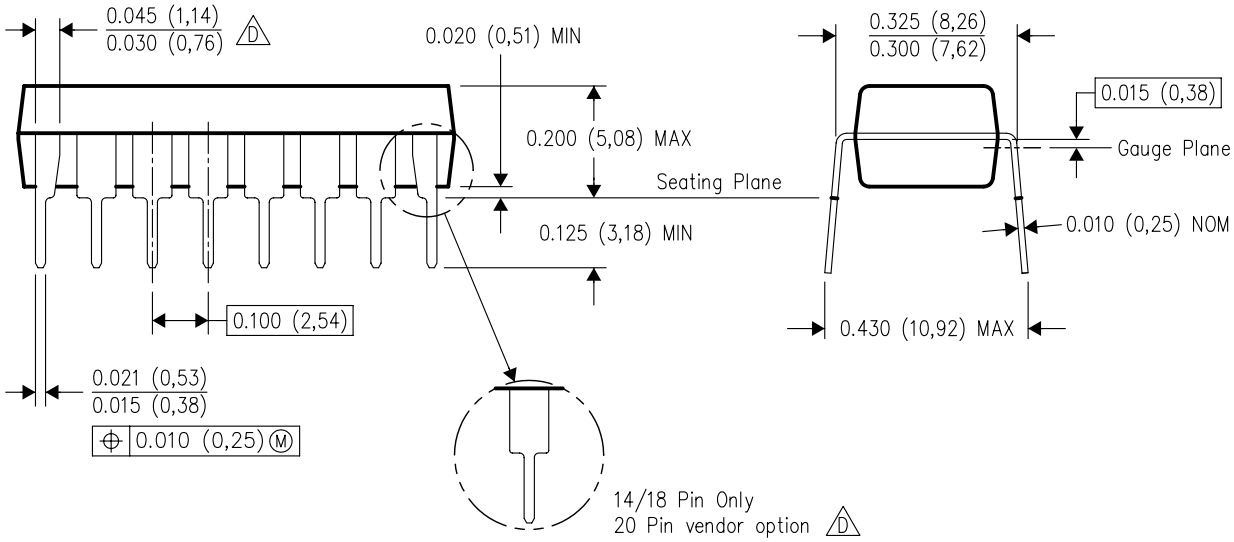
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



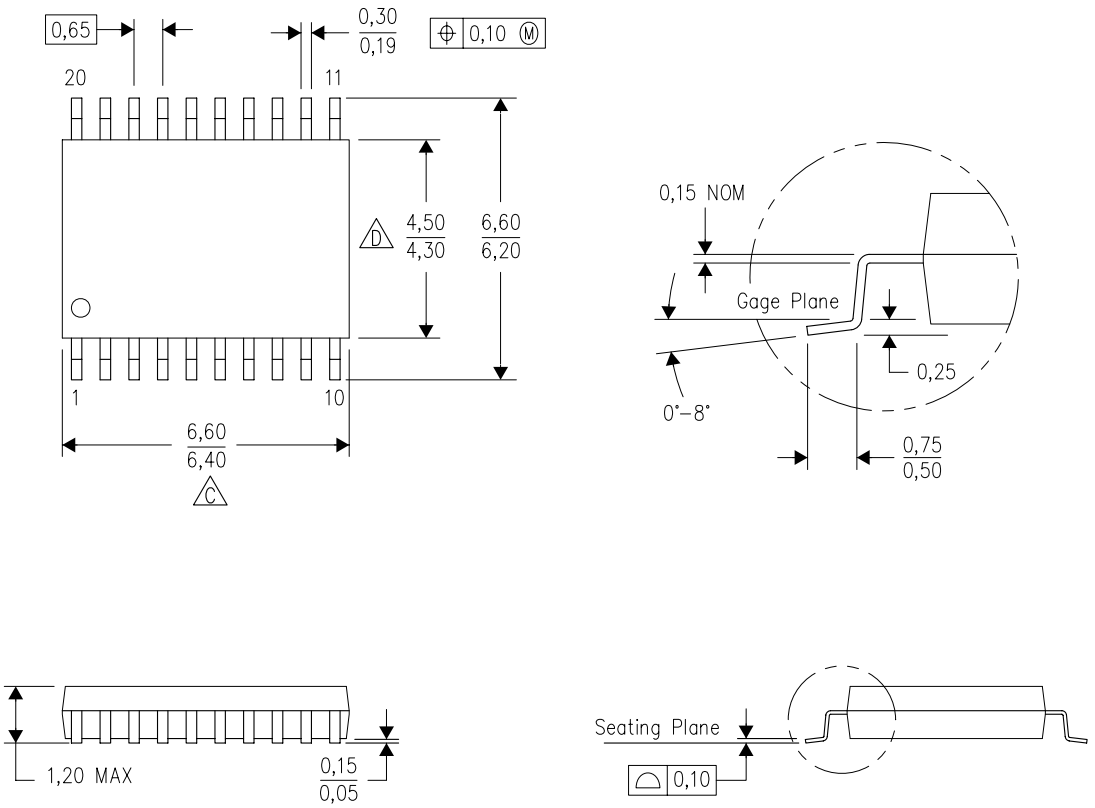
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

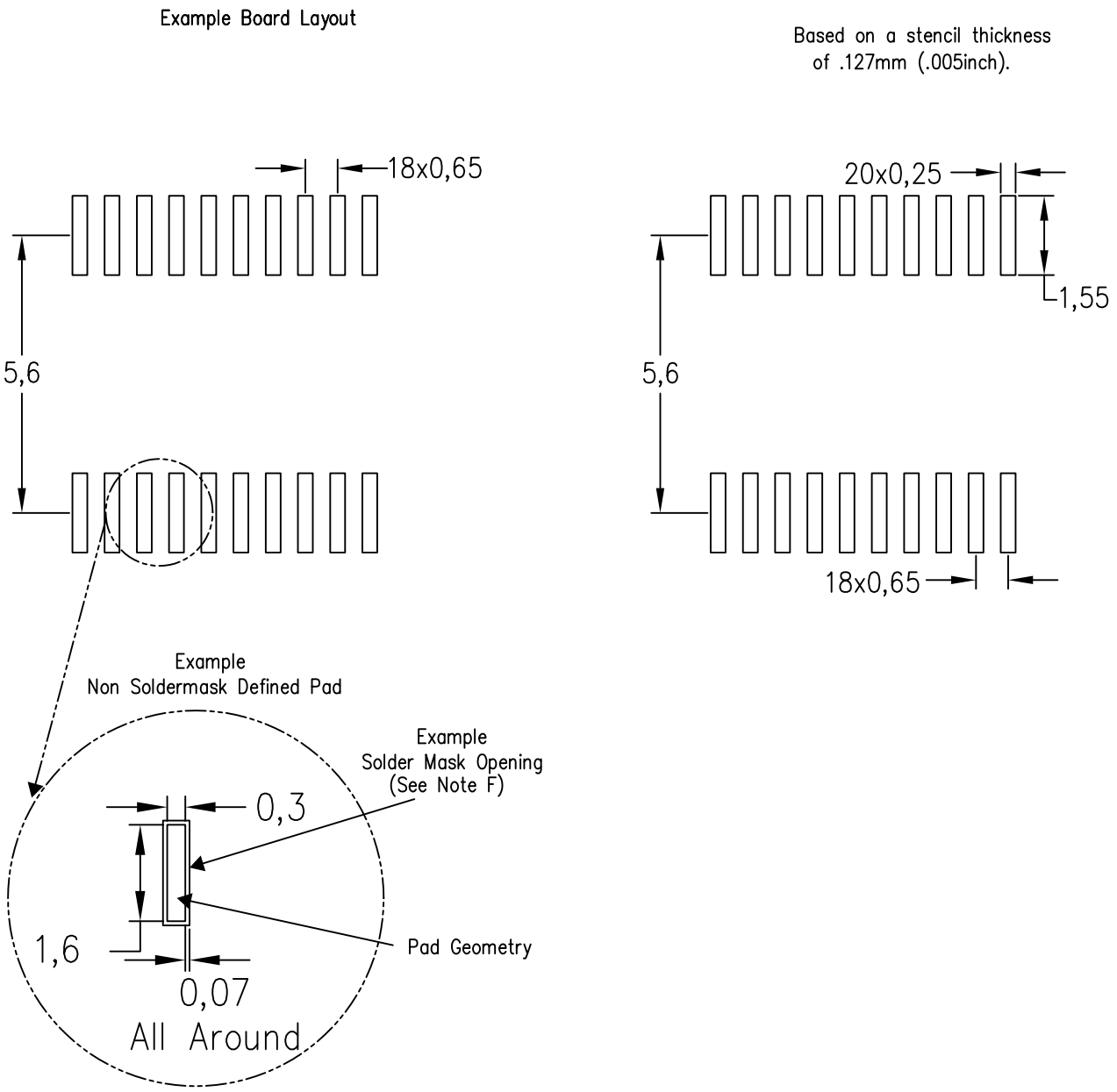
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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