Converting Oscillator Phase Noise to Time Jitter

by Walt Kester

INTRODUCTION

A low aperture jitter specification of an ADC is critical to achieving high levels of signal-to-noise ratios (SNR). (See References 1, 2, and 3). ADCs are available with aperture jitter specifications as low as 60-fs rms (AD9445 14-bits @ 125 MSPS and AD9446 16-bits @ 100 MSPS). Extremely low jitter sampling clocks must therefore be utilized so that the ADC performance is not degraded, because the total jitter is the root-sum-square of the internal converter aperture jitter and the external sampling clock jitter. However, oscillators used for sampling clock generation are more often specified in terms of phase noise rather than time jitter. The purpose of this discussion is to develop a simple method for converting oscillator phase noise into time jitter.

PHASE NOISE DEFINED

First, a few definitions are in order. Figure 1 shows a typical output frequency spectrum of a non-ideal oscillator (i.e., one that has jitter in the time domain, corresponding to phase noise in the frequency domain). The spectrum shows the noise power in a 1-Hz bandwidth as a function of frequency. Phase noise is defined as the ratio of the noise in a 1-Hz bandwidth at a specified frequency offset, f_m, to the oscillator signal amplitude at frequency f_O.

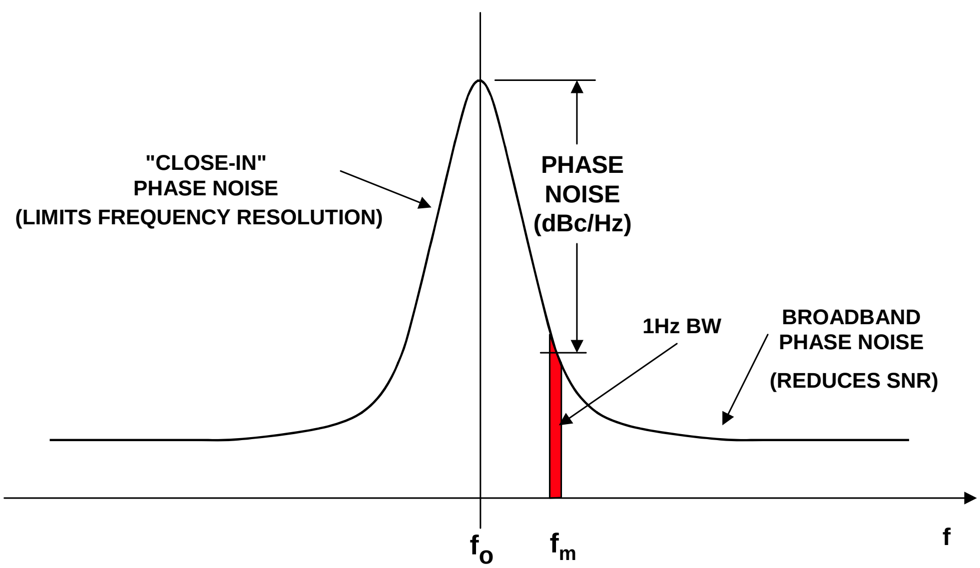


Figure 1: Oscillator Power Spectrum Due to Phase Noise

The sampling process is basically a multiplication of the sampling clock and the analog input signal. This is multiplication in the time domain, which is equivalent to convolution in the frequency domain. Therefore, the spectrum of the sampling clock oscillator is convolved with the input and shows up on the FFT output of a pure sinewave input signal (see Figure 2).

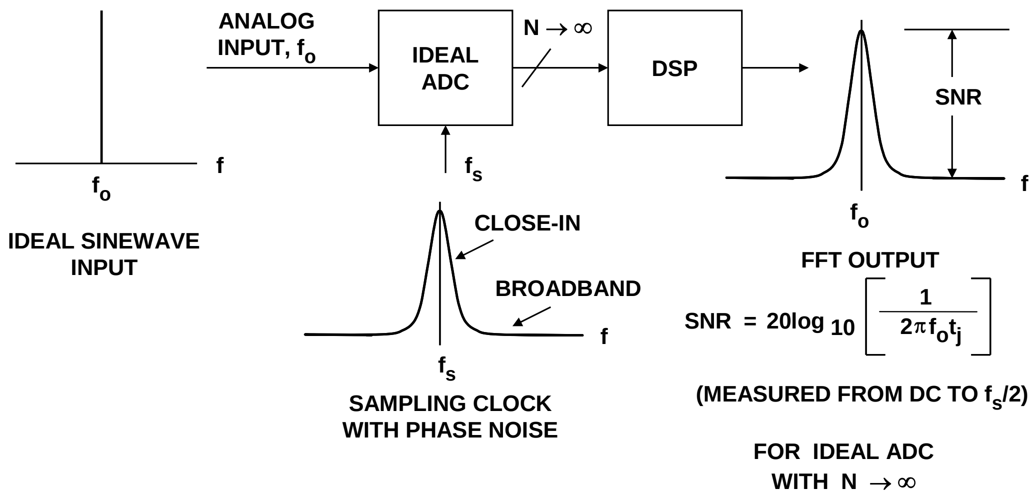


Figure 2: Effect of Sampling Clock Phase Noise Ideal Digitized Sinewave

The "close-in" phase noise will "smear" the fundamental signal into a number of frequency bins, thereby reducing the overall spectral resolution. The "broadband" phase noise will cause a degradation in the overall SNR as predicted by Eq. 1 (Reference 1 and 2):

$$\mathrm{SNR} = 20\log_{10}\left[\frac{1}{2\pi f t_j}\right]. \qquad \text{Eq. 1}$$

It is customary to characterize an oscillator in terms of its single-sideband phase noise as shown in Figure 3, where the phase noise in dBc/Hz is plotted as a function of frequency offset, f_m, with the frequency axis on a log scale. Note the actual curve is approximated by a number of regions, each having a slope of $1/f^{x}$, where x = 0 corresponds to the "white" phase noise region (slope = 0 dB/decade), and x = 1 corresponds to the "flicker" phase noise region (slope = –20 dB/decade). There are also regions where x = 2, 3, 4, and these regions occur progressively closer to the carrier frequency.

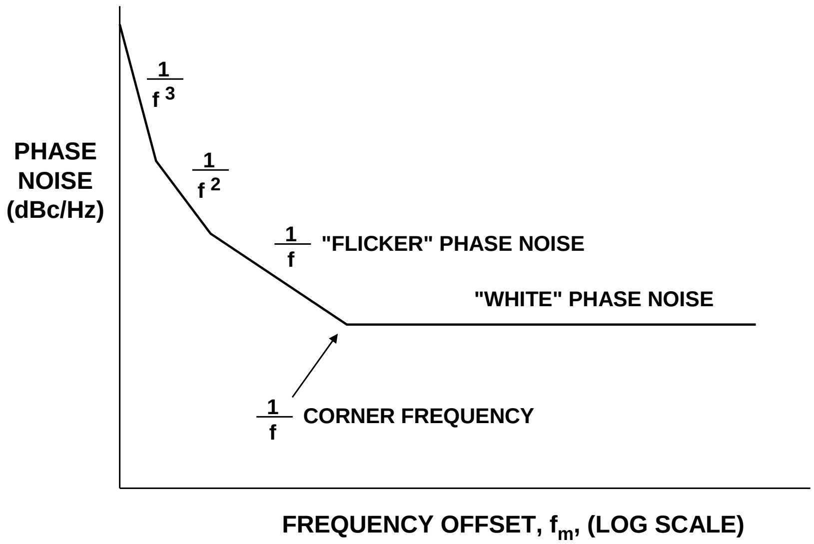


Figure 3: Oscillator Phase Noise in dBc/Hz vs. Frequency Offset

Note that the phase noise curve is somewhat analogous to the input voltage noise spectral density of an amplifier. Like amplifier voltage noise, low 1/f corner frequencies are highly desirable in an oscillator.

We have seen that oscillators are typically specified in terms of phase noise, but in order to relate phase noise to ADC performance, the phase noise must be converted into jitter. In order to make the graph relevant to modern ADC applications, the oscillator frequency (sampling frequency) is chosen to be 100 MHz for discussion purposes, and a typical graph is shown in Figure 4. Notice that the phase noise curve is approximated by a number of individual line segments, and the end points of each segment are defined by data points.

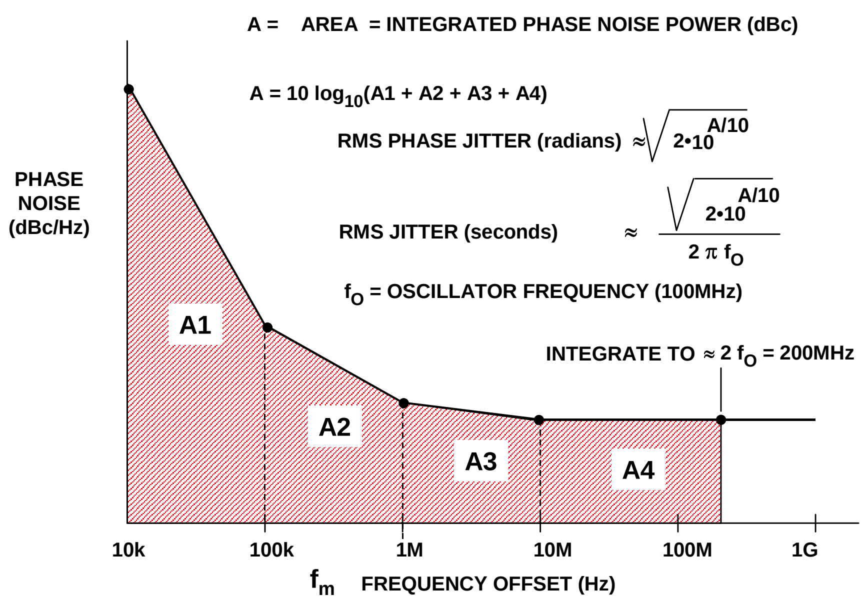


Figure 4: Calculating Jitter from Phase Noise

CONVERTING PHASE NOISE TO JITTER

The first step in calculating the equivalent rms jitter is to obtain the integrated phase noise power over the frequency range of interest, i.e., the area of the curve, A. The curve is broken into a number of individual areas (A1, A2, A3, A4), each defined by two data points. Generally speaking, the upper frequency range for the integration should be twice the sampling frequency, assuming there is no filtering between the oscillator and the ADC input. This approximates the bandwidth of the ADC sampling clock input.

Selecting the lower frequency for the integration also requires some judgment. In theory, it should be as low as possible to get the true rms jitter. In practice, however, the oscillator specifications generally will not be given for offset frequencies less than 10 Hz, or so—however, this will certainly give accurate enough results in the calculations. A lower frequency of integration of 100 Hz is reasonable in most cases, if that specification is available. Otherwise, use either the 1-kHz or 10-kHz data point.

One should also consider that the "close-in" phase noise affects the spectral resolution of the system, while the broadband noise affects the overall system SNR. Probably the wisest approach is to integrate each area separately as explained below and examine the magnitude of the jitter contribution of each area. The low frequency contributions may be negligible compared to the broadband contribution if a crystal oscillator is used. Other types of oscillators may have significant jitter contributions in the low frequency area, and a decision must be made regarding their importance to the overall system frequency resolution.

The integration of each individual area yields individual power ratios. The individual power ratios are then summed and converted back into dBc. Once the integrated phase noise power is known, the rms phase jitter in radians is given by the equation (see References 3-7 for further details, derivations, etc.),

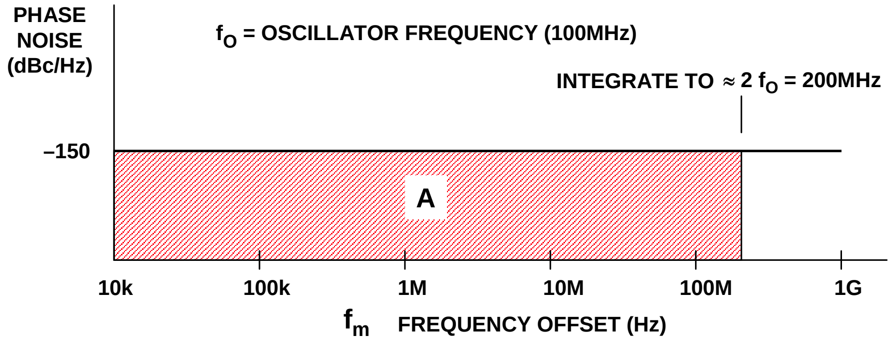
$$\text{RMS Phase Jitter (radians)} = \sqrt{2 \cdot 10^{A/10}}\,, \qquad \text{Eq. 2}$$

and dividing by $2\pi f_O$ converts the jitter in radians to jitter in seconds:

$$\text{RMS Phase Jitter (seconds)} = \frac{\sqrt{2 \cdot 10^{A/10}}}{2\pi\, f_O}\,. \qquad \text{Eq. 3}$$

It should be noted that computer programs and spreadsheets are available online to perform the integration by segments and calculate the rms jitter, thereby greatly simplifying the process (References 8, 9).

Figure 5 shows a sample calculation which assumes only broadband phase noise. The broadband phase noise chosen of –150 dBc/Hz represents a reasonably good signal generator specification, so the jitter number obtained represents a practical situation. The phase noise of –150 dBc/Hz (expressed as a ratio) is multiplied by the bandwidth of integration (200 MHz) to obtain the integrated phase noise of –67 dBc. Note that this multiplication is equivalent to adding the quantity 10 $\log_{10}$[200 MHz – 0.01 MHz] to the phase noise in dBc/Hz. In practice, the lower frequency limit of 0.01 MHz can be dropped from the calculation, as it does not affect the final result significantly. A total rms jitter of approximately 1 ps is obtained using Eq. 3.



$$A = -150\text{dBc} + 10\log_{10}\left[200\times10^{6} - 0.01\times10^{6}\right] = -150\text{dBc} + 83\text{dB} = -67\text{dBc}$$

$$\text{RMS PHASE JITTER (radians)} \approx \sqrt{2\cdot10^{A/10}} = 6.32\times10^{-4}\ \text{radians}$$

$$\text{RMS JITTER (seconds)} = \frac{\text{RMS PHASE JITTER (radians)}}{2\,\pi\, f_O} = 1\text{ps}$$

Figure 5: Sample Jitter Calculation Assuming Broadband Phase Noise

Crystal oscillators generally offer the lowest possible phase noise and jitter, and some examples are shown for comparison in Figure 6. All the oscillators shown have a typical 1/f corner frequency of 20 kHz, and the phase noise therefore represents the white phase noise level. The two Wenzel oscillators are fixed-frequency and represent excellent performance (Reference 9). It is difficult to achieve this level of performance with variable frequency signal generators, as shown by the –150 dBc specification for a relatively high quality generator.

- **Wenzel ULN Series*** **–174dBc/Hz @ 10kHz+**
- **Wenzel Sprinter Series,** **–165dBc/Hz @ 10kHz+**
- **High Quality Signal Generator** **–150dBc/Hz @ 10kHz+**

- **Thermal noise floor of resistive source in a matched system @ +25°C = –174dBm/Hz**
- **0dBm = 1mW = 632mV p-p into 50Ω**
- *** An oscillator with an output of +13dBm (2.82V p-p) into 50Ω with a phase noise of –174dBc/Hz has a noise floor of +13dBm – 174dBc = –161dBm, 13dB above the thermal noise floor**

(Wenzel ULN and Sprinter Series Specifications and Pricing Used with Permission of Wenzel Associates)

Figure 6: 100-MHz Oscillator Broadband Phase Noise Floor Comparisons (Wenzel ULN and Sprinter Series Specifications and Pricing used with Permission of Wenzel Associates)

At this point, it should be noted that there is a theoretical limit to the noise floor of an oscillator determined by the thermal noise of a matched source: –174 dBm/Hz at +25°C. Therefore, an oscillator with a +13-dBm output into 50 Ω (2.82-V p-p) with a phase noise of –174 dBc/Hz has a noise floor of –174 dBc + 13 dBm = –161 dBm. This is the case for the Wenzel ULN series as shown in Figure 6.

Figure 7 shows the jitter calculations from the two Wenzel crystal oscillators. In each case, the data points were taken directly for the manufacturer's data sheet. Because of the low 1/f corner frequency, the majority of the jitter is due to the "white" phase noise area. The calculated values of 64 fs (ULN-Series) and 180 fs represent extremely low jitter. For informational purposes, the individual jitter contributions of each area have been labeled separately. The total jitter is the root-sum-square of the individual jitter contributors.

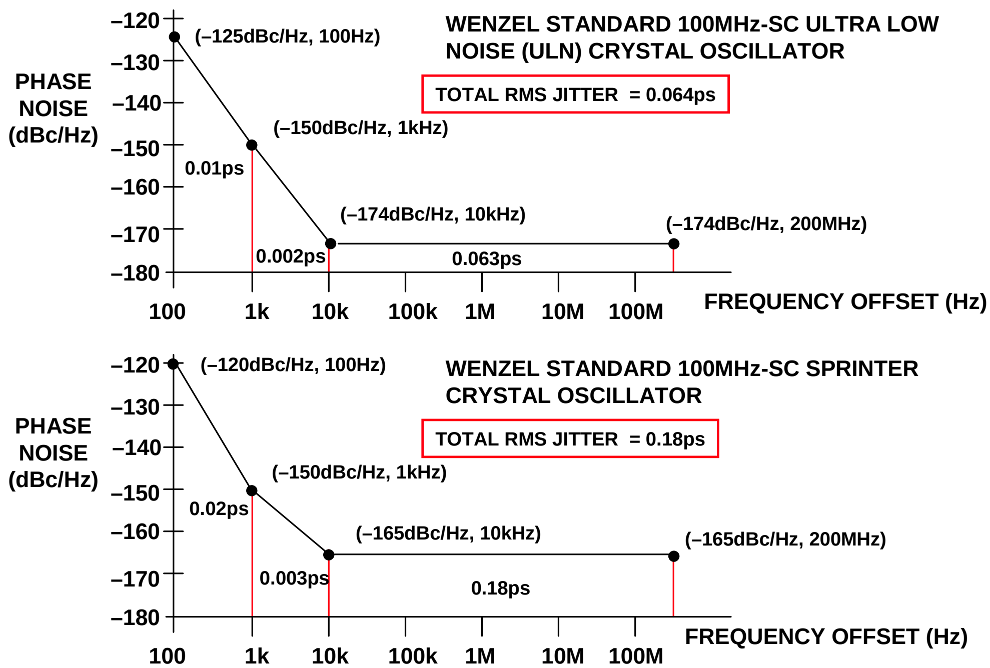


Figure 7: Jitter Calculations for Low Noise 100-MHz Crystal Oscillators (Phase Noise Data used with Permission of Wenzel Associates)

In system designs requiring low jitter sampling clocks, the costs of low noise dedicated crystal oscillators is generally prohibitive. An alternative solution is to use a phase-locked-loop (PLL) in conjunction with a voltage-controlled oscillator to "clean up" a noisy system clock as shown in Figure 8. There are many good references on PLL design (see References 10-13, for example), and we will not pursue that topic further, other than to state that using a narrow bandwidth loop filter in conjunction with a voltage-controlled crystal oscillator (VCXO) typically gives the lowest phase noise. As shown in Figure 8, the PLL tends to reduce the "close-in" phase noise while at the same time, reducing the overall phase noise floor. Further reduction in the white noise floor can be obtained by following the PLL output with an appropriate bandpass filter.

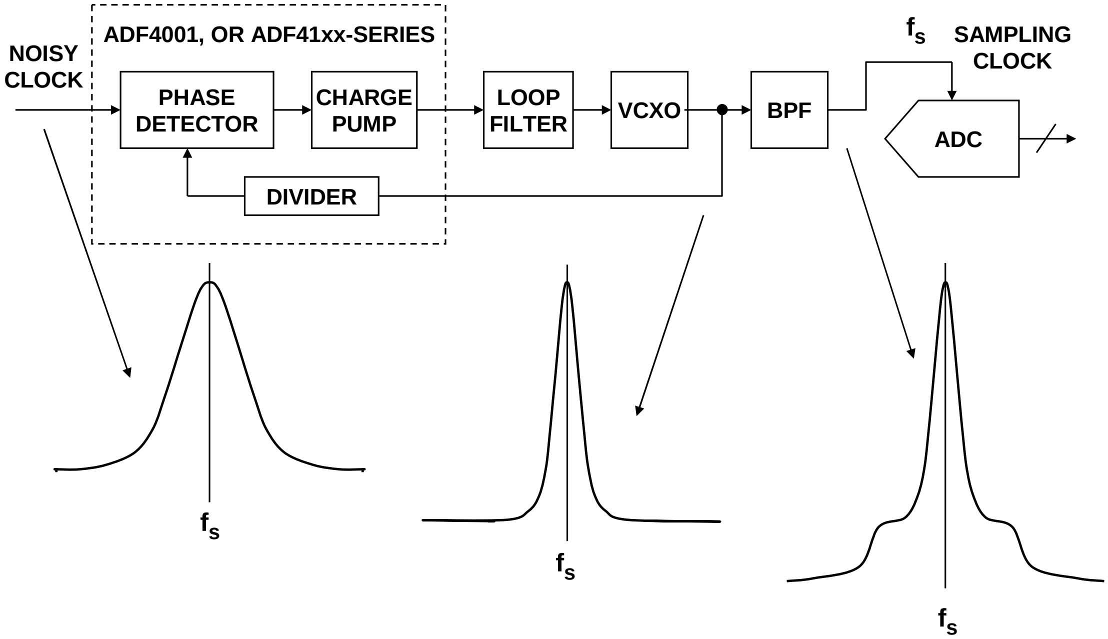


Figure 8: Using a Phase-Locked Loop (PLL) and Bandpass Filter to Condition a Noisy Clock Source

The effect of enclosing a free-running VCO within a PLL is shown in Figure 9. Notice that the "close-in" phase noise is reduced significantly by the action of the PLL.

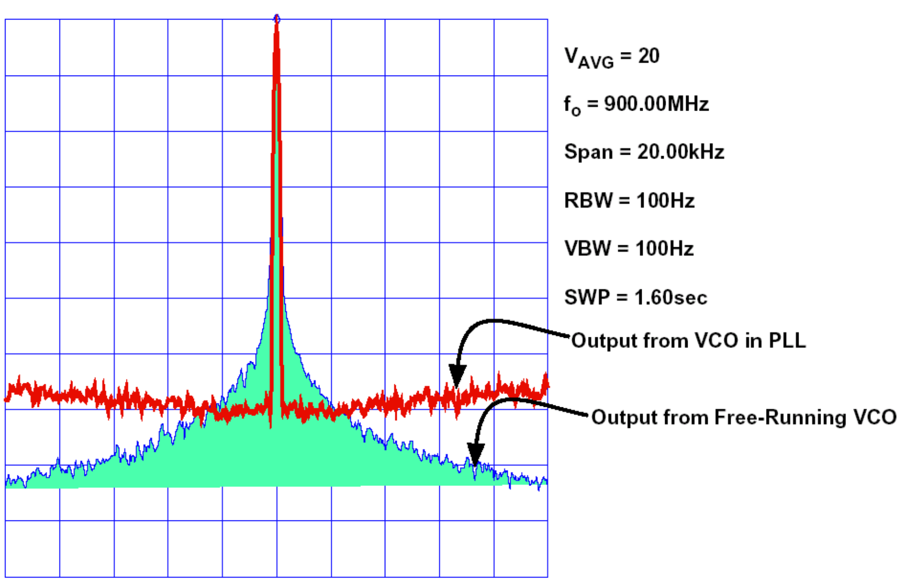


Figure 9: Phase Noise for a Free-Running VCO and a PLL-Connected VCO

Analog Devices offers a wide portfolio of frequency synthesis products, including DDS systems, N, and fractional-N PLLs. For example, the ADF4360 family are fully integrated PLLs complete with an internal VCO. With a 10-kHz bandwidth loop filter, the phase noise of the ADF4360-1 2.25-GHz PLL is shown in Figure 10, and the line-segment approximation and jitter calculations shown in Figure 11. Note that the rms jitter is only 1.57 ps, even with a non-crystal VCO.

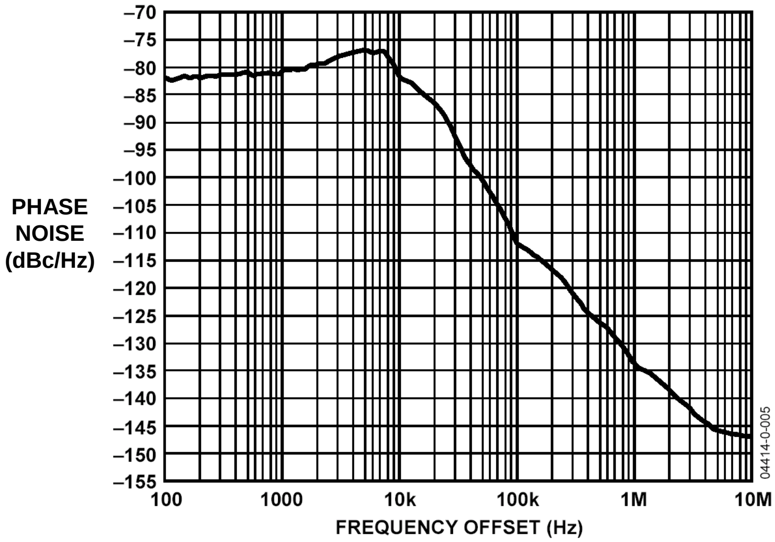


Figure 10: Phase Noise for ADF4360-1 2.25-GHz PLL with Loop Filter BW = 10 kHz

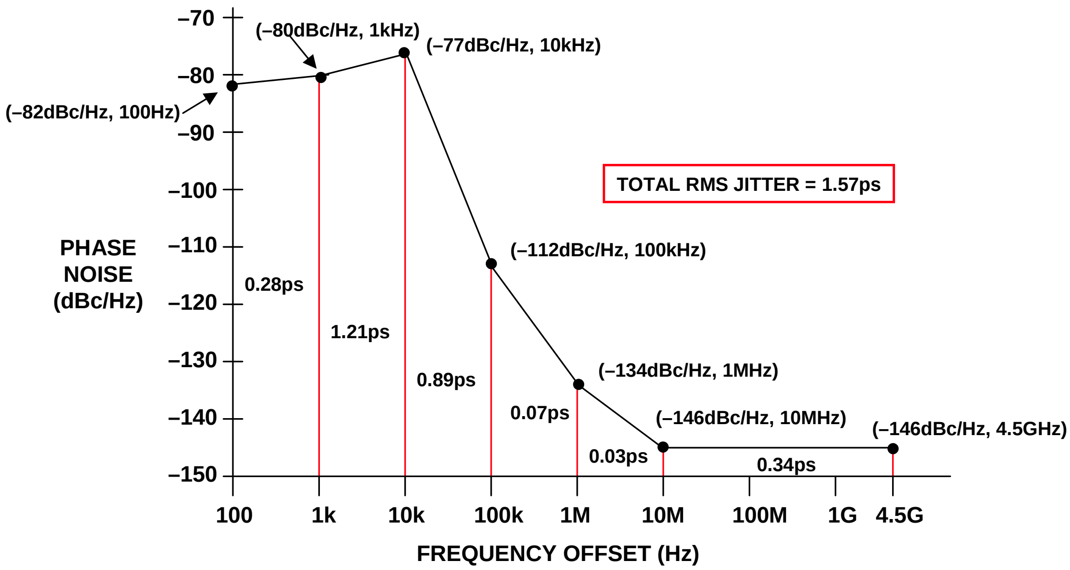


Figure 11: Line Segment Approximation to ADF4360-1, 2.25-GHz PLL Phase Noise Showing Jitter

Historically, PLL design relied heavily on textbooks and application notes to assist in the design of the loop filter, etc. Now, with Analog Devices free downloadable ADIsimPLL® software, PLL design is much easier. To start, choose a circuit by entering the desired output frequency range, and select a PLL, VCO, and a crystal reference. Once the loop filter configuration has been selected, the circuit can be analyzed and optimized for phase noise, phase margin, gain, spur levels, lock time, etc., in both the frequency and time domain. The program also performs the rms jitter calculation based on the PLL phase noise, thereby allowing the evaluation of the final PLL output as a sampling clock.

SUMMARY

Sampling clock jitter can be disastrous to the SNR performance of high performance ADCs. Although the relationship between SNR and jitter is well known, most oscillators are specified in terms of their phase noise. This article has shown how to convert phase noise into jitter so that the SNR degradation can be easily calculated.

Although not as good as relatively expensive stand alone crystal oscillators, modern PLLs using crystal VCOs (along with suitable filtering) can achieve jitter performance suitable for all but the most demanding requirements.

The entire problem of clock distribution has become much more critical because of low jitter requirements. Analog Devices is now offering a line of clock distribution ICs to serve these needs (www.analog.com/clocks).

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