FEATURES
Low current consumption: 1.95 mA typical
High phase frequency detector rate: 140 MHz
Hardware pin-programmable clock multiplication ratios:
  1x/5x/10x
Lock detect indicator
Power-down mode (0.8 μA typical)
8-lead MSOP package: 4.9 mm × 3.0 mm

APPLICATIONS
Low jitter clock generation
Low bandwidth (BW) jitter attenuation
Low frequency phase-locked loops (PLLs)
Frequency translation
Oven controlled crystal oscillator (OCXO) frequency multipliers
Phase lock clean high frequency references to 10 MHz equipment

GENERAL DESCRIPTION
Together with an external loop filter and a voltage controlled crystal oscillator (VCXO), the HMC1031 forms a complete clock generator solution targeted at low frequency jitter attenuation and reference clock generation applications.

The HMC1031 features a low power integer N divider, supporting divide ratios of 1, 5, and 10, which is controlled via external hardware pins and requires no serial port.

The integrated phase detector and charge pump are capable of operating at up to 140 MHz, and a maximum VCXO input of 500 MHz ensures frequency compliance with a wide variety of system clocks and VCXOs.

Additional features include an integrated lock detect indicator available on a dedicated hardware pin, and a built in power-down mode.

The HMC1031 is housed in an 8-lead MSOP package.
HMC1031* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS
View a parametric search of comparable parts.

EVALUATION KITS
• HMC1031MS8E Evaluation Board

DOCUMENTATION
Data Sheet
• HMC1031: 0.1 MHz to 500 MHz Clock Generator with Integer N PLL Data Sheet

TOOLS AND SIMULATIONS
• ADIsimPLL™

REFERENCE MATERIALS
Quality Documentation
• HMC Legacy PCN: MS##, MS##E and MS##G,MS##GE packages - Relocation of pre-existing production equipment to new building
• Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

DESIGN RESOURCES
• HMC1031 Material Declaration
• PCN-PDN Information
• Quality And Reliability
• Symbols and Footprints

DISCUSSIONS
View all HMC1031 EngineerZone Discussions.

SAMPLE AND BUY
Visit the product page to see pricing options.

TECHNICAL SUPPORT
Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK
Submit feedback for this data sheet.

This page is dynamically generated by Analog Devices, Inc., and inserted into this data sheet. A dynamic change to the content on this page will not trigger a change to either the revision number or the content of the product data sheet. This dynamic page may be frequently modified.
TABLE OF CONTENTS

- Features .............................................................................................. 1
- Applications ....................................................................................... 1
- Functional Block Diagram .............................................................. 1
- General Description ......................................................................... 1
- Revision History ............................................................................... 2
- Specifications ..................................................................................... 3
  - Electrical Specifications ............................................................... 3
  - Absolute Maximum Ratings ............................................................ 4
  - ESD Caution .................................................................................. 4
- Pin Configuration and Function Descriptions ............................. 5
  - Interface Schematics..................................................................... 6
  - Typical Performance Characteristics ..............................................7
- Applications Information .............................................................. 10
  - Jitter Attenuation ........................................................................ 10
  - Frequency Translation .................................................................. 10
- Loop Bandwidths with HMC1031 ........................................... 10
- Using VCOs/VCXOs with Negative Tuning Slope ................. 10
- Lock Detector ............................................................................. 10
- Printed Circuit Board (PCB) .................................................... 11
- Outline Dimensions ....................................................................... 13
- Ordering Guide .......................................................................... 13

REVISION HISTORY

10/15—v02.0215 to Rev. C

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

- Changed MS8E to MSOP and VCO Input to VCOIN...Throughout
- Changes to Features Section............................................................ 1
- Changes to Figure 3, Figure 4, and Figure 6 ................................. 6
- Deleted GND Interface Schematic; Renumbered Sequentially.. 7
- Change to Figure 17 ......................................................................... 8
- Changes to Lock Detector Section ............................................... 10
- Changes to Figure 25...................................................................... 12
- Updated Outline Dimensions....................................................... 13
- Changes to Ordering Guide.......................................................... 13
## ELECTRICAL SPECIFICATIONS

\( T_A = 25^\circ \text{C}, \) \( VCC = 3.3 \text{ V}, \) unless otherwise specified.

### Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER SUPPLY VOLTAGE</td>
<td></td>
<td>2.7</td>
<td>3.3</td>
<td>3.5</td>
<td>V</td>
</tr>
<tr>
<td>OPERATING TEMPERATURE</td>
<td></td>
<td>(-40)</td>
<td>+27</td>
<td>+85</td>
<td>(^{\circ}\text{C})</td>
</tr>
<tr>
<td>FREQUENCY(^1)</td>
<td>Reference Input(^2)</td>
<td>0.1</td>
<td>3.5</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>VCO Input</td>
<td></td>
<td>40</td>
<td>1.65</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>CHARGE PUMP Current</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>Output Range(^3)</td>
<td></td>
<td>0.2 to (VCC - 0.4)</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>INPUT Voltage Swing (Reference and VCOIN inputs)(^1)</td>
<td>Externally ac-coupled to the chip(^2)</td>
<td>122</td>
<td>3.5</td>
<td></td>
<td>V p-p</td>
</tr>
<tr>
<td>REFIN, VCOIN DC Bias</td>
<td>0.5 \times VCC approximately</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Duty Cycle</td>
<td></td>
<td>40</td>
<td>60</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Impedance at 50 MHz</td>
<td>Applicable to REFIN and VCOIN pins</td>
<td></td>
<td>3600(</td>
<td>4)</td>
<td></td>
</tr>
<tr>
<td>DIVIDE RATIOS</td>
<td>VCO/VCXO feedback divider</td>
<td>1/5/10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FIGURE OF MERIT (FOM)(^4)</td>
<td>Floor</td>
<td>(-212)</td>
<td>(-208)</td>
<td>(-204)</td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Flicker</td>
<td>(-254)</td>
<td>(-252)</td>
<td>(-248)</td>
<td>dBC/Hz</td>
<td></td>
</tr>
<tr>
<td>PHASE AND FLICKER NOISE Flicker Noise (PN(_{\text{FLICK}}))</td>
<td>(PN_{\text{FLICK}} = \text{Flicker FOM} + 20\log(f_{\text{VCXO}}) - 10\log(f_{\text{OFFSET}}))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phase Noise Floor (PN(_{\text{FLOOR}}))</td>
<td>(PN_{\text{FLOOR}} = \text{Floor FOM} + 10\log(f_{PD}) + 20\log(f_{\text{VCXO}}/f_{PD}))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CURRENT Supply(^5)</td>
<td>100 MHz reference = VCXO, (VCC = 3.3 \text{ V})</td>
<td>1.95</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>(\text{VCC} = 3.0 \text{ V}, 25^\circ \text{C}, D0 = 0, D1 = 0)</td>
<td>0.05</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td></td>
<td>(\text{VCC} = 3.3 \text{ V}, 85^\circ \text{C})</td>
<td>0.8</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td></td>
<td>(\text{VCC} = 3.6 \text{ V}, 85^\circ \text{C})</td>
<td>1</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>LOCK DETECT OUTPUT CURRENT</td>
<td>CMOS output level</td>
<td>3</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

---

1 The REFIN and VCOIN inputs must be ac-coupled to the HMC1031. The peak input level must not exceed \(VCC + 0.4 \text{ V}\) with respect to GND.

2 The lower limit of operation, 0.1 MHz, is limited by off-chip ac coupling. Select the size of the ac coupling capacitor such that the impedance, relative to the 3.6 k\(\Omega\) input impedance of the device and any termination impedances on the evaluation board (50 \(\Omega\) by default), is insignificant.

3 The PLL may lock in the voltage range of 0.2 V to \(VCC - 0.4 \text{ V}\). However, the charge pump gain may be reduced. See Figure 14 for charge pump compliance.

4 See Figure 17 for additional supply current data. Base frequency: 100 MHz; base VCXO, 3.3 V; \(0.8 \text{ mA}/\text{V}\) to 1 mA/V; base phase frequency detector (PFD) current: 1.8 mA, 8 \(\mu\text{A}/\text{MHz}\); base divider current: 1.15 mA, 15 \(\mu\text{A}/\text{MHz}\). For example, the device current for a 10 MHz reference and 50 MHz VCXO at 3.0 V VCC can be calculated as: \(\Delta \text{PFD current} = (10 - 100) \times (8 \times 10^{-6}) = -0.72 \text{ mA}, \Delta \text{DIV current} = (50 - 100) \times (15 \times 10^{-6}) = -0.75 \text{ mA}, \text{device current} = (1.8 - 0.72) + (1.15 - 0.75) = 1.48 \text{ mA at 3.3 V VCC}. \)

5 In power-down mode, the REFIN/VCOIN inputs and charge pump outputs are tristated. The power-down leakage current is measured without any signal applied to the HMC1031.
### ABSOLUTE MAXIMUM RATINGS

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC to GND</td>
<td>−0.3 V to +3.6 V</td>
</tr>
<tr>
<td>D0, D1 Pins to GND</td>
<td>−0.3 V to +3.6 V</td>
</tr>
<tr>
<td>Maximum REFIN Input Voltage</td>
<td>VCC + 0.4 V</td>
</tr>
<tr>
<td>Maximum VCOIN Input Voltage</td>
<td>VCC + 0.4 V</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>125°C</td>
</tr>
<tr>
<td>Maximum Peak Reflow Temperature (MSL1)</td>
<td>260°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>0.2°C/mW</td>
</tr>
<tr>
<td>Reflow Soldering</td>
<td></td>
</tr>
<tr>
<td>Peak Temperature</td>
<td>260°C</td>
</tr>
<tr>
<td>Time at Peak Temperature</td>
<td>40 sec</td>
</tr>
<tr>
<td>ESD Sensitivity (Human Body Model (HBM))</td>
<td>Class 2</td>
</tr>
</tbody>
</table>

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

**ESD CAUTION**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 3. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>Supply Voltage (3.3 V Typical).</td>
</tr>
<tr>
<td>2</td>
<td>REFIN</td>
<td>Reference Input. REFIN is an externally ac-coupled reference frequency input.</td>
</tr>
<tr>
<td>3</td>
<td>LKDOP</td>
<td>Lock Detect Output, CMOS Drive.</td>
</tr>
<tr>
<td>4, 5</td>
<td>D0, D1</td>
<td>Integer N Division Ratio Selection. D0 and D1 are the CMOS inputs used to specify the integer N division ratio. See Table 4.</td>
</tr>
<tr>
<td>6</td>
<td>VCOIN</td>
<td>Voltage Controlled Oscillator Input. VCOIN is an ac-coupled VCO/VCXO input.</td>
</tr>
<tr>
<td>7</td>
<td>CP</td>
<td>Charge Pump Output.</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>Ground.</td>
</tr>
</tbody>
</table>

Table 4. Frequency Multiplication Truth Table

<table>
<thead>
<tr>
<th>D0</th>
<th>D1</th>
<th>PLL Feedback Division Ratio (N)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Power-down mode</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Divide by 1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Divide by 5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Divide by 10</td>
</tr>
</tbody>
</table>

1 Set by SW1 in the evaluation PCB schematic (see Figure 24).
INTERFACE SCHEMATICS

Figure 3. REFIN Interface Schematic

Figure 4. LKDOP Interface Schematic

Figure 5. D0, D1 Interface Schematic

Figure 6. VCOIN Interface Schematic

Figure 7. CP Interface Schematic
TYPICAL PERFORMANCE CHARACTERISTICS

$T_a = 25^\circ C$, $VCC = 3.3$ V, unless otherwise specified.

Figure 8. 10 MHz to 100 MHz with Noisy Reference Phase Noise; Loop Filter Value: $C8 = 4.7$ nF, $R7 = 1.2$ kΩ, $C9 = 62$ μF, Loop Filter BW = 8 Hz, VCXO = 100 MHz Crystek CVHD-950

Figure 9. 10 MHz to 100 MHz with Very Noisy Reference Phase Noise; Loop Filter Value: $C8 = 4.7$ nF, $R7 = 1.2$ kΩ, $C9 = 62$ μF; Loop Filter BW = 8 Hz; VCXO = 100 MHz Crystek CVHD-950

Figure 10. Phase Error During Lock Time for Divide by 5; 10 MHz Input; 50 MHz Output; Loop BW = 100 Hz; Refer to Loop Filter Configuration 2 in Table 5

Figure 11. 10 MHz to 50 MHz with Noisy Reference Phase Noise; Loop Filter Value: $C8 = 220$ nF, $R7 = 3.3$ kΩ, $C9 = 2.2$ μF; Loop Filter BW = 50 Hz, VCXO = Bliley V105ACACB, 50 MHz

Figure 12. Typical Closed-Loop Phase Noise, HMC1031 as Jitter Attenuator, Loop BW = 100 Hz; Refer to Loop Filter Configuration 2 in Table 5

Figure 13. Frequency Error During Lock Time for Divide by 5; 10 MHz Input; 50 MHz Output; Loop Bandwidth = 100 Hz; Refer to Loop Filter Configuration 2 in Table 5
Figure 14. Typical Source and Sink Current vs. Charge Pump Output Voltage

Figure 15. REFIN Input Power vs. Input Frequency

Figure 16. VCOIN Input Power vs. Input Frequency, Maximum Frequency Is Guaranteed in the Recommended Region of Operation Across Temperature and Process Variation

Figure 17. Current vs. Supply Voltage, Different Configurations

Figure 18. REFIN Input Voltage Swing vs. Input Frequency

Figure 19. VCOIN Input Voltage Swing vs. Input Frequency; Maximum Frequency Is Guaranteed in the Recommended Region of Operation Across Temperature and Process Variation
Figure 20. Flicker FOM

Figure 21. Floor FOM
APPLICATIONS INFORMATION

JITTER ATTENUATION
In some cases, reference clocks to the system may come from external noisy sources with high jitter. The HMC1031 can be used to attenuate this incoming jitter and distribute a clean clock in the system. In such a scheme, a narrow loop filter is selected for the HMC1031. The device frequency locks to the external VCXO, but the reference jitter is attenuated as defined by the set loop filter bandwidth. The final output frequency and phase noise characteristics outside the loop bandwidth is defined by the phase noise characteristics of the VCXO used. A low jitter clock reference yields better clocking performance and better LO performance of the RF PLL VCOs, and improves the SNR performance of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

FREQUENCY TRANSLATION
The reference clock in a test and measurement system or a communications system is often a high accuracy OCXO with excellent long-term stability. In some applications, the OCXO frequency must be multiplied up to a higher rate to drive the primary clock inputs in a system. The HMC1031 offers a very low power, small package and high performance method to multiply its incoming frequency in 1×, 5×, and 10× rates. Such multiplication is required because the higher reference clocks improve phase noise, ADC/DAC signal-to-noise ratio (SNR), clock generator jitter, and PHY bit error rates (BERs). In this scheme, the HMC1031 can be connected to an external low cost VCXO (for example, at 50 MHz or 100 MHz), and lock this external VCXO to the excellent long-term stability of the OCXO.

LOOP BANDWIDTHS WITH HMC1031
In typical jitter attenuation applications, an incoming reference clock is frequency locked with a narrow PLL loop bandwidth such that its incoming noise is filtered out by the PLL and VCXO combination. The out of band phase noise of the PLL follows the VCXO that it is locked to. A narrow PLL loop bandwidth ensures that the output jitter is determined by the VCXO (or any other type of high quality factor VCO) and not affected by the spectral noise of the incoming clock beyond the set loop bandwidth.

To facilitate narrow bandwidth loop filter configurations, the HMC1031 is designed to have a low charge pump current of 50 µA. This architecture offers advantages in low power consumption and loop filter design. Typically, narrow loop filter bandwidths require large filter capacitors. Due to the low charge pump current design of the HMC1031, smaller loop filter capacitor sizes can be used to implement narrow loop filters. Note that the HMC1031 is designed to operate in loop bandwidths of only a few kilohertz in its widest loop bandwidth configuration.

USING VCOs/VCXOs WITH NEGATIVE TUNING SLOPE
In its typical configuration, the HMC1031 works with any VCO/VCXO that has a positive tuning slope. For any VCO/VCXO with negative tuning slope, that is, when the frequency decreases with increasing tuning voltage, connect the loop filter ac ground to VCC instead of GND.

LOCK DETECTOR
The lock detector measures the arrival times between the divided VCO edge and reference edge appearing at the phase detector. When this offset becomes greater than approximately 6 ns, the lock detector indicates an out of lock condition. Any leakage current on the CP output causes a phase offset between the two edges. Due to the relatively small 50 µA charge pump current, the HMC1031 is sensitive to leakage currents and may indicate a false out of lock condition if the leakage current from the charge pump (Pin 7) to ground is too high.

Leakage currents include dc current through the loop filter capacitors and/or dc current into the VCO tuning voltage pin, V_TUNE. It is recommended to use low leakage, loop filter multilayer ceramic capacitors (MLCCs) and careful VCO selection to maximize V_TUNE resistance. The maximum acceptable leakage is dependent on the phase detector operating frequency and can be calculated as follows:

\[
\frac{I_{\text{LEAKAGE}}}{I_{\text{CP}}} = \frac{3 \text{ ns}}{t_{\text{PD}}}
\]

where:
- \(I_{\text{LEAKAGE}}\) is the total leakage current in µA.
- \(I_{\text{CP}}\) is the charge pump current in µA (set to 50 µA).
- \(t_{\text{PD}}\) is the reference frequency period in ns.

Internal delays reduce the available lock detector range from 6 ns to 3 ns.
For example, to guarantee correct lock detector operation with a 10 MHz reference ($t_{PD} = 100$ ns) and no leakage into the VCO $V_{TUNE}$ pin, the total capacitor leakage must be less than 1.5 $\mu$A. A typical MLCC 33 nF, 25 V loop filter capacitor has approximately 0.5 nA of leakage (Murata GRM155R71E333KA88).

**PRINTED CIRCUIT BOARD (PCB)**

Use a sufficient number of via holes to connect the top and bottom ground planes (see Figure 23). The evaluation circuit board design is available from Analog Devices upon request.

*Figure 23. Evaluation PCB*
Table 5. Loop Filter Configuration

<table>
<thead>
<tr>
<th>Configuration</th>
<th>$f_{\text{REF}}$ (MHz)</th>
<th>$f_{\text{VCO}}$ (MHz)</th>
<th>Divider</th>
<th>Bandwidth (Hz)</th>
<th>C8</th>
<th>R7</th>
<th>C9</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>100</td>
<td>10</td>
<td>10</td>
<td>220</td>
<td>7.5 kΩ</td>
<td>4.7 µF</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>50</td>
<td>5</td>
<td>100</td>
<td>100</td>
<td>5.6 kΩ</td>
<td>1 µF</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td>50</td>
<td>5</td>
<td>2000</td>
<td>300 pF</td>
<td>100 kΩ</td>
<td>3.9 nF</td>
</tr>
</tbody>
</table>
OUTLINE DIMENSIONS

Figure 25. 8-Lead Mini Small Outline Package [MSOP] (HRM-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
<th>Branding2</th>
</tr>
</thead>
<tbody>
<tr>
<td>HMC1031MS8E</td>
<td>−40°C to +85°C</td>
<td>8-Lead Mini Small Outline Package [MSOP]</td>
<td>HRM-8-1</td>
<td>H1031</td>
</tr>
<tr>
<td>HMC1031MS8ETR</td>
<td>−40°C to +85°C</td>
<td>8-Lead Mini Small Outline Package [MSOP]</td>
<td>HRM-8-1</td>
<td>H1031</td>
</tr>
<tr>
<td>EVAL01-HMC1031MS8E</td>
<td></td>
<td>HMC1031MS8E Evaluation PCB</td>
<td></td>
<td>XXXX</td>
</tr>
</tbody>
</table>

1 E = RoHS Compliant Part.
2 XXXX is the four-digit lot number.