Output Terminations for SiT9102/9002/9107 LVPECL, LVDS, CML, and HCSL Differential Drivers

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1 Introduction

SiTime offers a wide selection of output differential signaling types to facilitate various clock applications. The supported signaling types are LVPECL (Low-Voltage Positive Emitter-Coupled Logic), LVDS (Low-Voltage Differential Signaling), CML (Current Mode Logic), and HCSL (High-Speed Current Steering Logic).

Differential signals typically have fast rise times, e.g., between 100ps and 400ps, which causes even short traces to behave as transmission lines. These traces have to be terminated properly for minimal reflections, optimal signal integrity, and the least EMI.

The traces in most high-speed differential applications are designed either as two 50Ω uncoupled transmission lines (each 50Ω to GND plane), or as one 100Ω coupled differential trace pair.

Minimal reflections are achieved when the traces are terminated on one or both ends with impedances that match the trace impedance. (Refer to Appendix A for more details about source and/or load termination strategies.) In addition to impedance matching, the termination networks impact the DC bias and AC voltage swings at the receivers. This application note describes each output type and the recommended termination methods for proper impedance matching, DC biasing, and AC swing levels.

2 LVPECL Output

The SiTime LVPECL outputs use current-mode drivers, primarily to accommodate multiple signaling formats. Two types of LVPECL outputs are provided, “LVPECL0” and “LVPECL1”, each suitable for different set of termination methodologies that are either commonly used or would provide specific benefits in some custom applications. SiTime generally recommends LVPECL0 and LVPECL1 as below:

1. LVPECL0: when the device outputs are AC-coupled to the load termination circuit
2. LVPECL1: when the device outputs are DC-coupled to the load termination circuit.

The uses of LVPECL0 and LVPECL1 are not restricted to the two cases just listed. They may also be used in special applications, such as double termination. The following sections provide further detail about using LVPECL0 and LVPECL1 outputs and the associated termination recommendations.

2.1 LVPECL1 Output

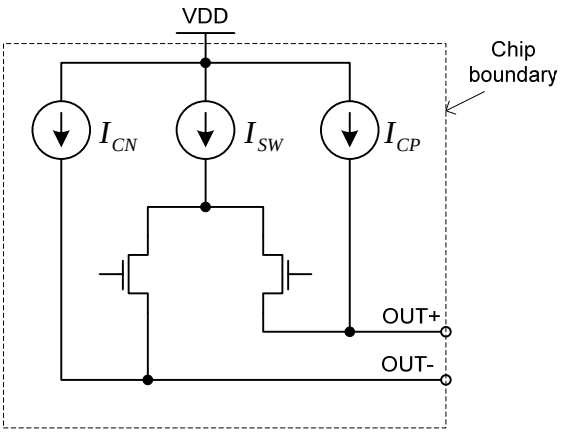


Figure 1: SiTime LVPECL1 driver output structure

The structure of the SiTime LVPECL1 driver is shown in Figure 1. Each output is driven by two current sources: a switched 16 mA current source (I_{SW}) and a dedicated constant 6 mA current source (I_{CP} or I_{CN}). Typically, the outputs are terminated to VDD-2V via 50Ω resistors. When an output is high, it will source 22 mA of current (16 mA + 6 mA). When it is low, it will drive only 6 mA of current. Consequently, the voltage developed across the 50Ω load resistor will vary nominally between 1.1V and 300 mV, thus creating a single-ended signal swing of 800mV.

This single-ended signal swing is only nominally 800mV. Since the output voltage is proportional to the value of the load resistor, large variations in resistor value may result in excessive variations in voltage swing. For systems sensitive to signal swings beyond the nominal range, the use of 1% precision resistors is recommended.

Figure 2 shows the typical termination network for DC-coupled load terminated LVPECL outputs. The outputs are terminated with a 50Ω resistor to the termination voltage (VT), providing good impedance match to the transmission line. In Figure 2, the receiver input impedance is assumed to be high (greater than 1kohm or so). Therefore, the 50Ω resistors should be placed as close to the receiver as possible to avoid the formation of unterminated stubs, which can cause signal integrity issues. Note that the receiver may be connected in two ways: either directly to the termination circuit, or through AC-coupled capacitors. The latter is used when the receiver biasing is different from what the termination circuit provides.

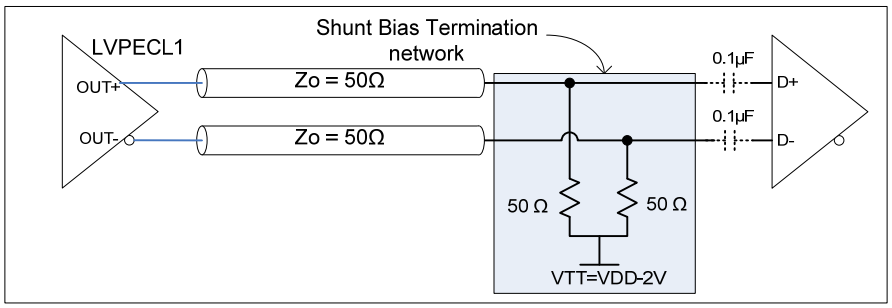
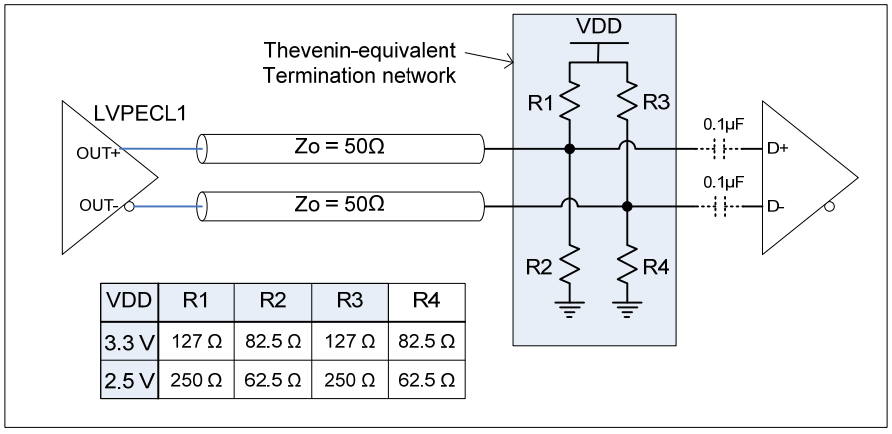


Figure 2: LVPECL with DC-coupled parallel Shunt load termination

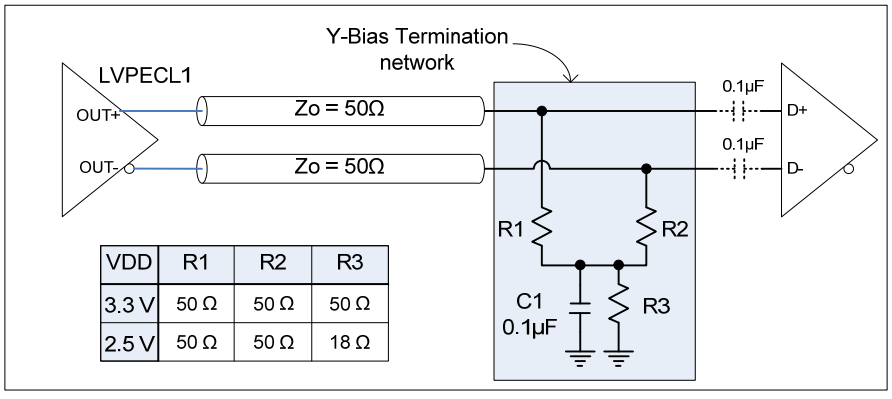
For SiTime LVPECL current drivers, output impedance is in the range of several K-ohms while Z_o is close to 50Ω for most traces and cables. This results in a source reflection coefficient (Γ_S) close to 100% (see Appendix A), thus reflecting back virtually all of the signal that has been reflected from the load. Fortunately, the round-trip reflection signal is small because the majority of the signals will be absorbed by the load due to its low reflection coefficient (Γ_L).

In applications where a separate termination voltage is not readily available, pull-up and pull-down resistors forming a Thevenin Equivalent network can terminate the 50Ω transmission line. Such a network effectively establishes a 50Ω impedance to the termination voltage of VDD-2V at the receiver. This termination method is shown in Figure 3; note that the resistor values are different for 3.3V and 2.5V supply voltages. As in Shunt load termination, the AC-coupled capacitors may used between the termination network and the receiver where needed.



VDD	R1	R2	R3	R4
3.3 V	127 Ω	82.5 Ω	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω	250 Ω	62.5 Ω

Figure 3: LEVPECL DC-coupled load termination with Thevenin Equivalent network



VDD	R1	R2	R3
3.3 V	50 Ω	50 Ω	50 Ω
2.5 V	50 Ω	50 Ω	18 Ω

Figure 4: LVPECL with Y-Bias termination

In most case the Thevenin Equivalent termination works well, but it can be sensitive to the power supply noise if there is any significant mismatch between traces or between the resistor networks on each side of the differential pair, or if the receiver is too sensitive to common-mode noise. Figure 4 shows the Y-Bias termination network, which provides an effective termination voltage of VDD-2V without requiring either connection to VDD or access to an additional termination voltage source. The termination voltage is generated by the sum of differential pair

currents passing through the R3. The capacitance C1 is used to create AC ground at the termination voltage. As in previous cases, the AC-coupled capacitors may be used between the termination network and the receiver where needed.

Parallel load termination may not provide the best signal integrity for some LVPECL applications, including the following cases:

1. When it is difficult to place the termination network close to the receiver, i.e., within 0.1in to 0.3in from the receiver. In such cases, the traces connecting the termination network to the receiver will appear as a stub and will degrade signal integrity at the receiver inputs.
2. When there are large capacitive loads at the receiver inputs. Such capacitive loads will reduce the termination impedance when the fast edges of the signal reach the receiver, causing a large load reflection coefficient. This reflection will return to the load with little attenuation after being reflected at the source. The rule of thumb is that the termination mismatch becomes significant if $3.T_r/(\pi.C_L)$ is less than 50Ω, where T_r is the 20%-to-80% rise time, and C_L is the load capacitance.

In such scenarios, source termination is a better option, which can be implemented by placing any of the termination networks shown in Figure 2, Figure 3, and Figure 4 close to the driver. (Refer to Appendix A for general details on source termination.)

Note: The termination networks in Figure 2, Figure 3, and Figure 4 cannot be used for source termination with the low-impedance LVPECL (open emitter) drivers. Such drivers require series impedances for source termination (see Appendix A).

For most applications, a single termination at the source or load minimizes the reflections sufficiently. In some situations, it may not be possible to achieve good matching with load or source termination alone. An effective strategy is double termination. Figure 5 shows an example of double termination for LVPECL signals. Any combination of termination networks shown in Figure 2, Figure 3, and Figure 4 can be used at the source and load with SiTime LVEPCL outputs. When using Y-Bias termination in double termination cases, the R3 should be 100Ω and 36Ω for 3.3V and 2.5V power supply voltages, respectively.

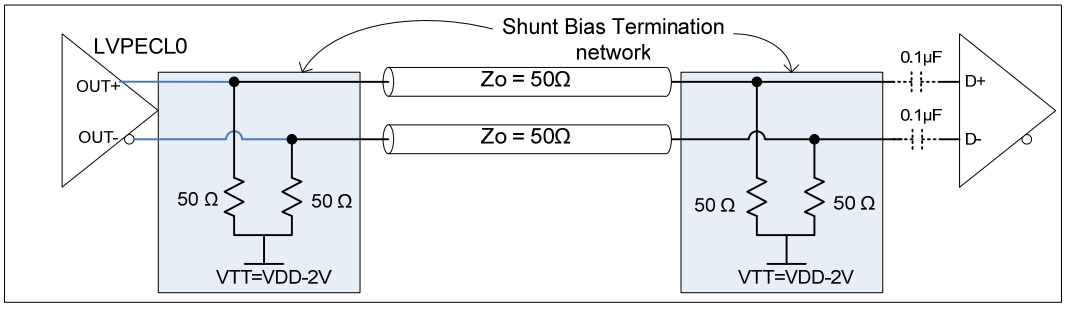


Figure 5: LVPECL double termination (source and load)

With the addition of the 50Ω termination at the source, a 25Ω equivalent load is presented to the LVPECL driver, reducing the differential signal swing from 1600 mV to 800 mV. If this signal level is insufficient for the receiver, the user can choose the LVPECL0 version of the oscillator with higher switched current drivers. The switched current sources (see Figure 1) in these

oscillators are enhanced from 16 mA to 22 mA, thus increasing the signal swing for a 25Ω load from 400 mV to 550 mV.

2.2 LVPECL0 Output

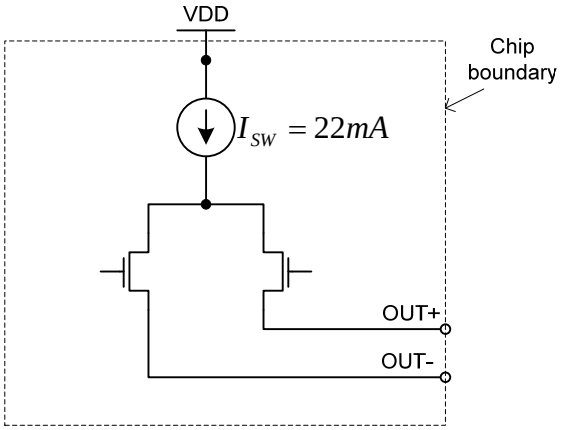


Figure 6: LVPECL0 driver output structure

The LVPECL0 driver output structure is shown in Figure 6. The LVPECL0 switched current, I_{SW}, is 22mA. This effectively increases the outputs' switching drive capacity from the LVPECL1 mode's 16mA to 22mA. One use of this mode is for LVPECL with an AC-coupled termination circuit, as described below.

An AC-coupled termination is often recommended when the LVPECL output drives a differential receiver with a termination voltage different from what the driver needs. As shown in Figure 7, a capacitor is used to block the DC path to the load termination and receiver, allowing the receiver to set its own termination voltage. In this example, the receiver inputs are biased by a 50Ω resistor to a termination voltage, which is determined by the receiver requirements. Since the capacitor blocks the DC path for the driver's outputs, additional 150Ω resistors are installed between the outputs and ground at the source to provide the required output DC current paths.

From the AC standpoint, the R1/R2 resistors at the source are in parallel with the 50Ω resistors at the load, resulting in a 37.5Ω equivalent load to the driver. To obtain the nominal LVPECL signal swings at the load, the user should choose the LVPECL0 output mode of SiT9102 with 22 mA current drivers, thus increasing the nominal signal swing to 825 mV.

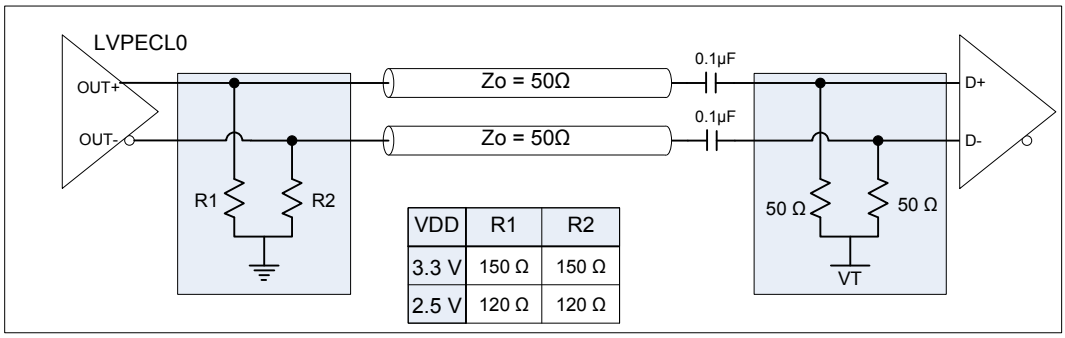


Figure 7: LVPECL0 in load terminated AC-coupled application

3 HCSL Output

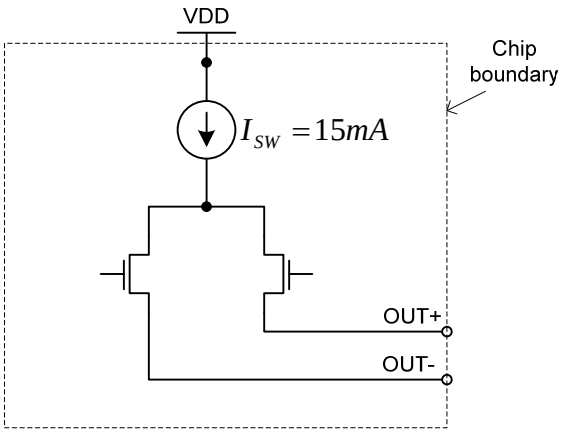


Figure 8: HCSL driver output structure

The HCSL output structure (see Figure 8) is driven by a 15 mA switched current source typically terminated to ground via a 50Ω resistor. The nominal signal swing is 750 mV. The HCSL interface is typically source-terminated with a 50Ω load as shown in Figure 9. The open-drain transistor at the output has fairly high impedance in the range of several kilo-ohms. From an AC standard point, the output transistor's impedance is parallel to the 50Ω load resistor, resulting in an equivalent resistance very close to 50Ω. Since the traces used in this interface have a characteristic impedance of 50Ω, any signal reflected from the load will be absorbed at the source. Typically, two small resistors, R1 and R2 (see Figure 9), are placed in series with the high-impedance driver. They function as an overshoot limiter by slowing down the rapid rise of current from the output, and have no impact on the impedance matching at the source. SiTime recommends 20Ω for these resistors.

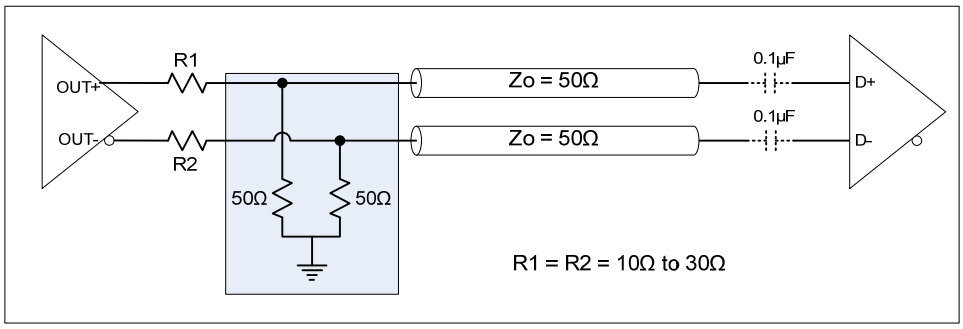


Figure 9: HCSL interface termination

4 LVDS Output

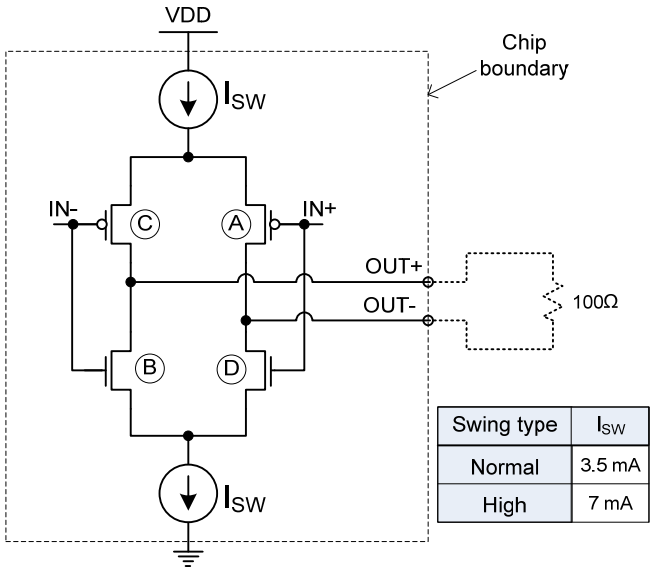


Figure 10: LVDS driver output structure

LVDS [1] is a high-speed digital interface suitable for many applications that require low power consumption and high noise immunity. LVDS uses differential signals with low voltage swings to transmit data at high rates. Figure 10 shows the output structure of an LVDS driver, consisting of a 3.5 mA nominal current source connected to differential outputs via a switching network. The outputs are typically attached to 100Ω differential transmission lines terminated with a 100Ω resistor at the receiver end. The resistor's impedance matches the impedance of the transmission lines and provides a current path for the signal. The common mode voltage is specified at 1.2V.

Signal switching is accomplished with four transistors labeled A, B, C, and D, respectively. Because the impedance of the receiver is typically high, virtually all of the current from the driver will flow through the 100Ω resistor, resulting in a voltage difference of 350 mV between the receiver inputs. In Figure 10, when the signal IN is low, transistors A and B will be turned on; the current will flow through transistor A and the 100Ω resistor, and return through transistor B. When signal IN is high, transistors C and D will be turned on; the current will flow through transistor C and the 100Ω resistor, and return through transistor D, resulting in -350mV voltage across the receiver.

For the receiver, the direction of the current flowing through the termination resistor determines whether a positive or negative differential voltage is registered. A positive differential voltage represents a logic high level, while a negative differential voltage represents a logic low level.

SiTime provides two types of LVDS output swings: normal and high. The "normal swing" version has a 3.5 mA current source while the "high swing" version features a 7 mA current source. The high swing version is designed to be used in double termination configurations. Both versions are available for 3.3V and 2.5V applications.

4.1 Termination Recommendations for DC-Coupled Applications

A LVDS interface with 100Ω differential traces is typically terminated at the receiver end with a 100Ω resistor across the differential inputs of the receiver (see Figure 11). Some receivers have incorporated the 100Ω resistor on-chip, eliminating the need for external termination.

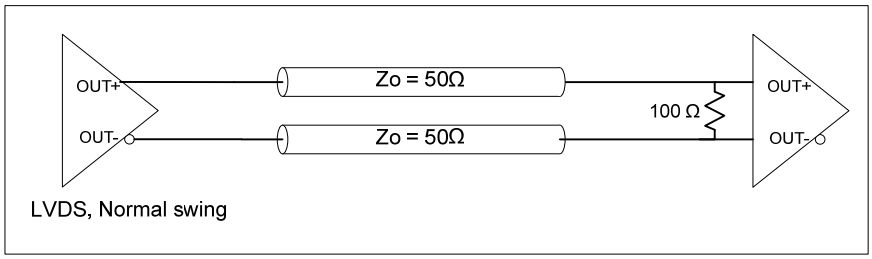


Figure 11: LVDS single DC termination at the load

For most applications, a single termination at the load is sufficient. In situations where the load reflection coefficient is relatively high, a double termination arrangement may reduce the overall round trip (see Figure 12). (Refer to Appendix A for more information on the uses of single and double termination arrangements.) With a 100Ω resistor at both the source and the load, the equivalent resistance at the output driver is reduced to 50Ω, causing the output signal swing to be cut in half. SiTime provides the high swing option for its LVDS drivers with 7 mA current drive to restore the differential signal swing to ±350 mV.

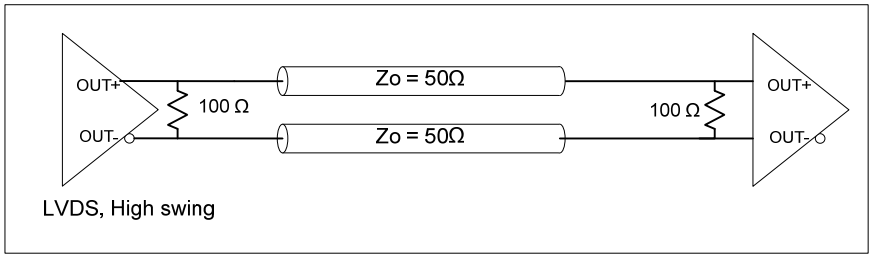


Figure 12: LVDS double DC termination

4.2 Termination Recommendations for AC-Coupled Applications

If the LVDS driver and the receiver are operating with different common mode voltages, then an AC termination is recommended. A capacitor is used to block the DC current path from the driver; in such cases, the receiver must implement its own input bias circuit.

AC coupling can be configured as either a single termination at the load or as a double termination. With a single load termination, as shown in Figure 13, the AC-coupled capacitors should be placed between termination resistor and the receiver for proper DC biasing of the driver. For double-terminated links, the AC-coupling capacitor can be placed before (Figure 14) or after (Figure 15) the load termination resistor. The high swing version may be used with the double termination.

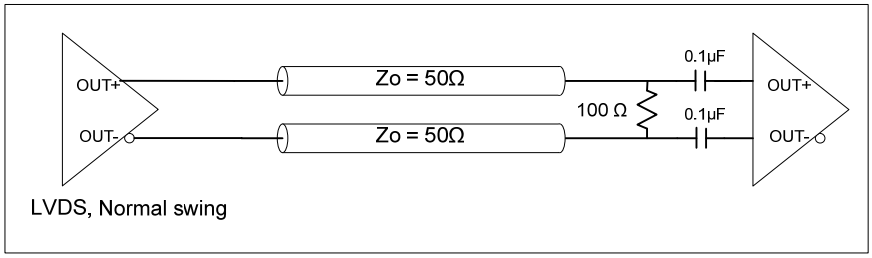


Figure 13: LVDS single AC termination at the load

The double terminations shown in Figure 14 and Figure 15 differ only in the position of the AC-coupling capacitor. The capacitor in Figure 14 is charged by the common mode current flowing through half the differential resistance, which is the equivalent of 50Ω. On the other hand, the capacitor in Figure 15 is charged by the current through the resistance of the receiver's inputs, which can be in the range of kilo-ohms. During clock start-up, the capacitor shown in Figure 14 will be charged much faster than that shown in Figure 15. Therefore, a valid clock signal will be available sooner to the receiver. If fast clock start-up is important, the configuration shown in Figure 14 is preferable.

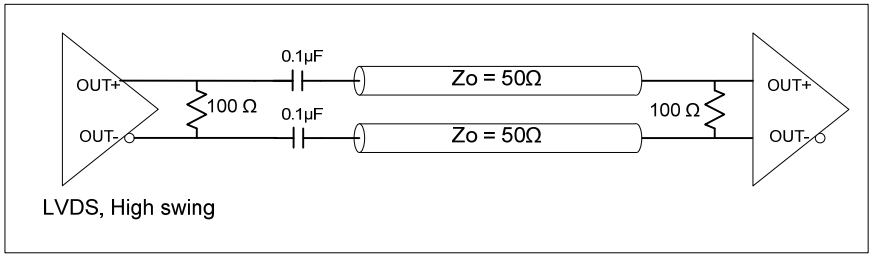


Figure 14: LVDS double AC termination with capacitor close to the source

In data transmission applications, the configuration shown in Figure 15 may be more advantageous. Because of its higher RC time constant, it can sustain data sequences with longer 1s and 0s without experiencing significant voltage droop.

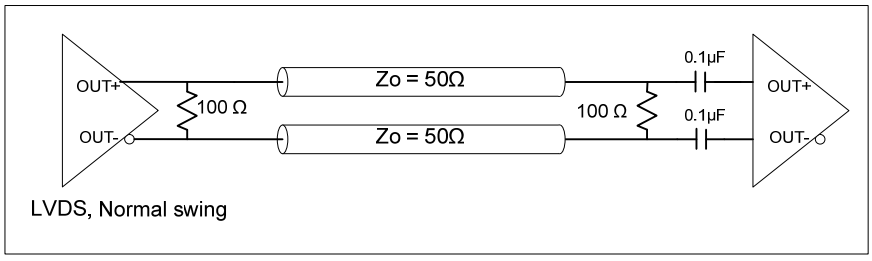


Figure 15: LVDS double AC termination with capacitor close to the load

5 CML Output

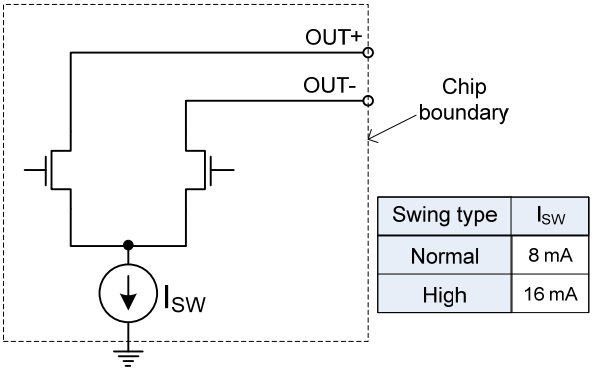


Figure 16: CML driver output structure

SiTime CML drivers are constructed with an NMOS open-drain differential pair and an 8 mA constant current source. The output structure is shown in Figure 16. Because the open-drain transistors are only capable of pulling down a signal, external pull-up resistors are needed. Voltage swing across a 50Ω resistor is typically 400 mV.

SiTime's CML clocks can operate at 3.3V, 2.5V, and 1.8V. Two output signal swing versions are supported: normal and high. The normal swing version is equipped with an 8 mA current source, while the high swing version has a 16 mA current source.

5.1 Termination Recommendations for DC-Coupled Applications

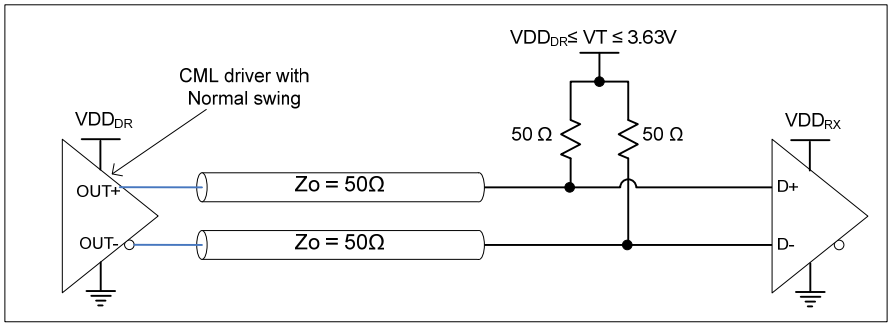


Figure 17: CML with single DC load termination

A typical CML termination is shown in Figure 17. The differential outputs are pulled up to a termination voltage. In most cases, the driver supply voltage (VDD_{DR}) is used for the VT. However, in applications where the driver and the receiver are operated at different VDDs, VT is typically set to the driver supply voltage or the higher of the two VDDs, as long as it does not exceed the maximum allowable voltage for the driver or the receiver.

For a double termination strategy, both the source and the load are typically terminated to the same VT, as shown in Figure 18. Because two 50Ω termination resistors are connected in parallel to the output, their equivalent resistance is reduced to 25Ω, causing a 50% reduction in the output swing. SiTime offers the CML high swing version with 16 mA current drivers to restore the signal swing back to 400mV.

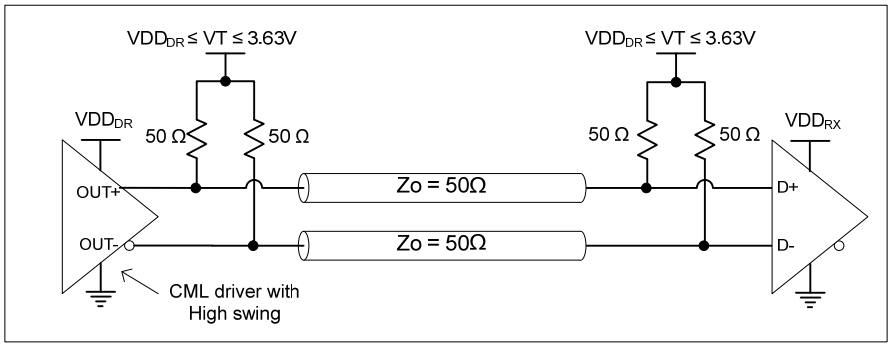


Figure 18: CML with double DC termination

5.2 Termination Recommendations for AC-Coupled Applications

AC termination should be used if the receiver requires a different input bias from what the termination provides. The DC path to the receiver is blocked by the capacitor, so the user must provide a separate bias circuit for the receiver inputs. In many cases, a single termination at the load end is sufficient (see Figure 18). The VT is typically the VDD of the driver.

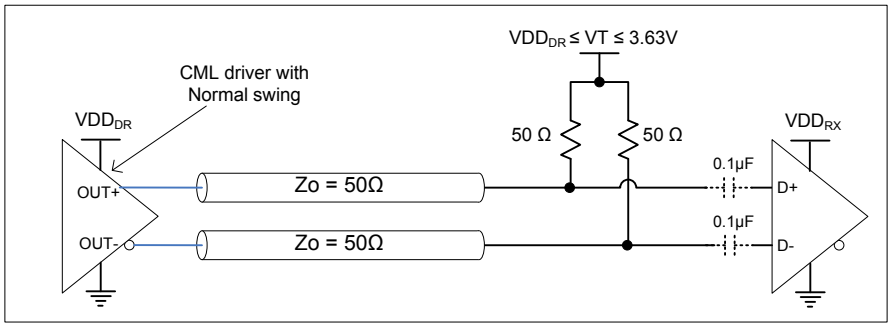


Figure 19: CML single AC termination at the load

For better signal integrity, double termination configurations, shown in Figure 20 and Figure 21, may be used. The CML high swing version may be used in double terminations to maintain a 400 mV signal swing. As in the discussion about AC coupling with LVDS links, the main difference between the AC coupling shown in Figure 20 and Figure 21 is the effective time constant for the common-mode signal. The first provides shorter time constants, which may be advantageous for getting stable signals faster in clock applications. The longer time constants shown in Figure 21 may be preferable in data-carrying links, to sustain data sequences with longer 1s and 0s without experiencing significant voltage droop.

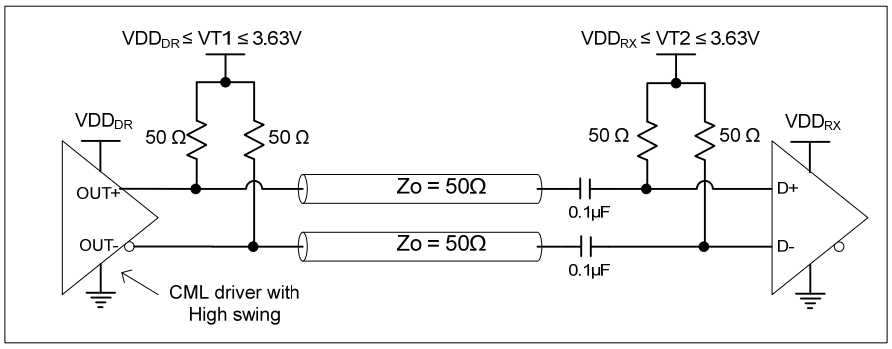


Figure 20: CML double AC termination with capacitor close to the source

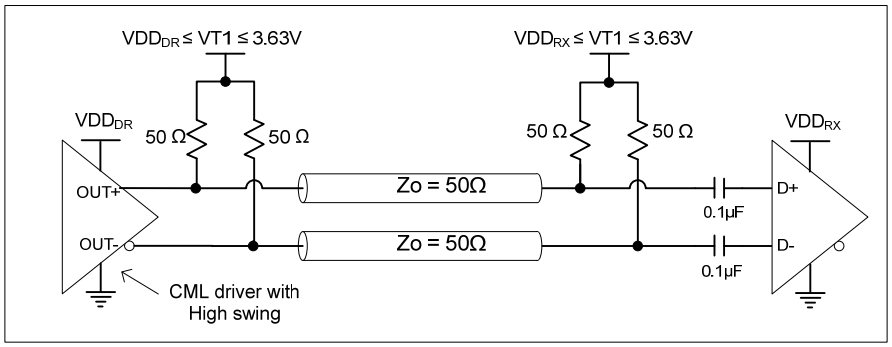


Figure 21: CML double AC termination with capacitor close to the load

5.3 CML-to-LVDS Termination Recommendations

CML signaling with SiTime differential oscillators provides unique features, which may be attractive in applications with non-CML receivers, such as LVDS. Such benefits include:

1. Lower current consumption than other signaling types. Under typical conditions, the current savings relative to LVDS is in the 22mA to 27mA range
2. 1.8V supply voltage support
3. Slightly lower jitter

The circuit shown in Figure 22 allows direct connection of the CML outputs to the LVDS inputs. The voltage divider R1/R2 generates an effective 1.5V termination voltage, while the 0.1 µF provides AC ground for the 50Ω termination resistors. SiTime CML outputs support termination voltages as low as 1.5V (±5%) with normal swing parts for all VDD options (VDD = 3.3V, 2.5V, and 1.8V). The penalty is typically a 10% increase in rise/fall times. Such termination voltage results in a 1.3V common mode to satisfy the LVDS receiver requirements. R1 and R2 values should be selected to obtain 1.5V at node VT:

$$VT = \frac{R2}{R1 + R2}\left(VDD - R1.I_{DC}\right), \qquad \text{Equation 1}$$

where $I_{DC} = 8mA$ represents the DC current going through the termination circuit (R1||R2). A reasonable choice is to remove R2, i.e., $R2 = \infty$, which leads to the following values for R1:

- VDD=3.3V → R1=225Ω, 1%
- VDD=2.5V → R1=125Ω, 1%
- VDD=1.8V → R1=37.5Ω, 1%

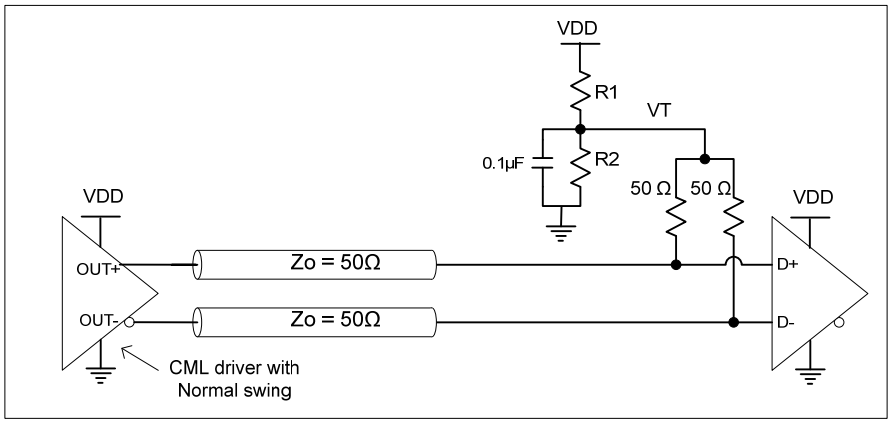


Figure 22: CML-to-LVDS Shunt termination network

Another method for connecting CML outputs to LVDS inputs is to decouple the DC levels using AC-coupling capacitors, as shown in Figure 23. The bias circuits, R1=R3 and R2=R4, should be designed to provide the LVDS offset voltage of 1.25V at the receiver. The termination resistors, AC-coupled capacitors, and the bias networks should be placed close to the receiver for best signal integrity. From an AC point of view, the bias network impedance is in parallel with the termination resistor. To avoid significant mismatch due to the bias networks, the R1||R2 should be great than 1kΩ.

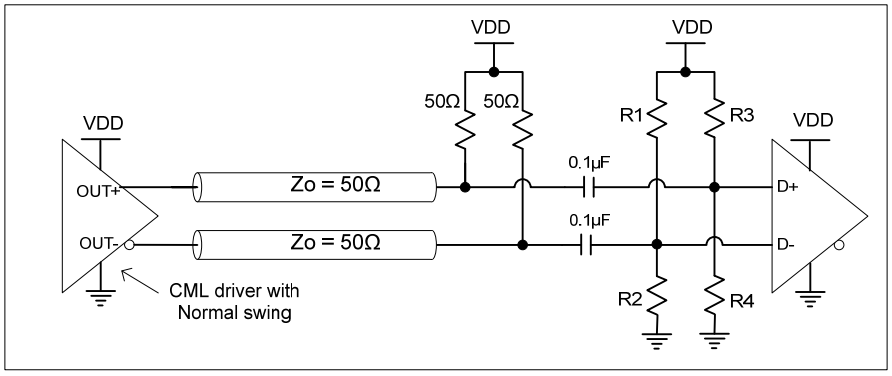


Figure 23: CML-to-LVDS interface with AC coupling and DC bias circuit

The AC coupling method shown in Figure 23 may also be used to interface CML outputs to LVPECL inputs provided that the bias networks are designed for the nominal offset of LVPECL circuits, which is typically VDD-1.3V.

6 Conclusion

This application note presented the SiT9102, SiT9002, and SiT9107 differential output driver structures and the most commonly used AC-coupled and DC-coupled termination recommendations for four types of differential outputs: LVPECL, HCSL, LVDS, and CML. Additionally, multiple current strength options in these clocks support double termination strategies without sacrificing signal swing voltages. With such a rich selection of output types, users can easily find the ones that fit their design requirements.

7 Reference

[1] Telecommunications Industry Association, *"Electrical Characteristics of low voltage differential signaling (LVDS) interface circuits"*, TIA/EIA-644-A standard specifications, February 2001.

8 Appendix A: Transmission Line Termination Impedance Matching

Any trace of a printed circuit board (PCB) or cable behaves as a transmission line when its electrical length is greater than half of the 20%-to-80% rise time of the signal that is being launched to the trace. Proper termination is an important factor for optimal signal integrity. This Appendix discusses source, load, and double termination strategies.

8.1 Load Termination

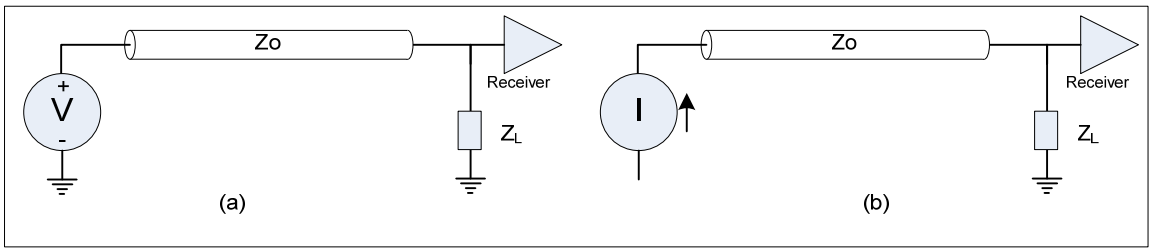


Figure 24: Transmission line parallel load termination

Figure 24 (a) and (b) show transmission lines terminated with parallel load impedance of Z_L and driven by a voltage or current signal. Once the signal reaches the load at the other side of the line, some of its energy will be absorbed by the load and the rest will reflect back to the source. The ratio of the reflected signal to the incident one is referred to as the reflection coefficient and is computed as below:

$$\Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o} \qquad \text{Equation 2}$$

If the load is terminated with the same impedance as the trace, i.e., $Z_L = Z_o$, then $\Gamma_L = 0$, which means no signal will reflect back. If the load impedance does not match that of the trace, some of the signal will reflect to the source. A fraction of the reflected signal will reflect back to the load depending on the source reflection coefficient, computed as below:

$$\Gamma_S = \frac{Z_S - Z_o}{Z_S + Z_o} \qquad \text{Equation 3}$$

The overall reflection seen at the load is the result of round-trip reflection through the transmission line, which can be computed using the round-trip reflection coefficient, Γ_{RT}, computed as below:

$$\Gamma_{RT} = \Gamma_S . \Gamma_L \qquad \text{Equation 4}$$

The round-trip reflection Γ_{RT} should be minimized for optimal signal integrity. A large value of Γ_{RT} can cause reduced signal margin, extra trigger edges in digital applications, or excessive ringing at load.

For the voltage driver in Figure 24(a), $Z_S = 0$, which leads to $\Gamma_S = -1$, while for the current driver in Figure 24(b), $Z_S = \infty$, which leads to $\Gamma_S = +1$. In both cases, all the energy of the signal reflected from the load will reflect back to the load, leading to $\Gamma_{RT} = -\Gamma_L$ and $\Gamma_{RT} = \Gamma_L$ for Figure 24(a) and Figure 24(b), respectively. Therefore, the load impedance should be matched well with that of the trace to avoid signal integrity issues.

8.2 Source Termination

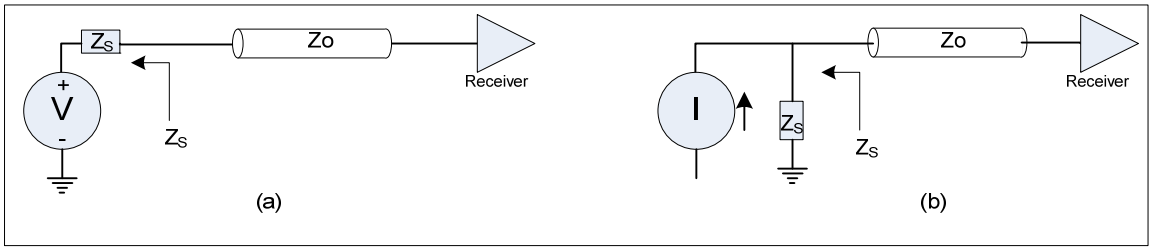


Figure 25: Transmission line source termination

In some applications, it is difficult to properly terminate the transmission line at the load, for example, due to uncontrolled impedances at the load or inability to place the termination close to the receiver circuit at the end of the line. In such cases, the source termination strategies shown in Figure 25(a) and (b) can be used. The receivers are assumed to have high impedance, which leads to a load reflection coefficient of 1 ($\Gamma_L = +1$). The signal will reflect to the source, where much of the energy gets absorbed by the source impedance when Z_S is matched to Z_o, and only a small portion will reflect back to the load. The round-trip reflection coefficient will be $\Gamma_{RT} = \Gamma_S$.

8.3 Double Termination

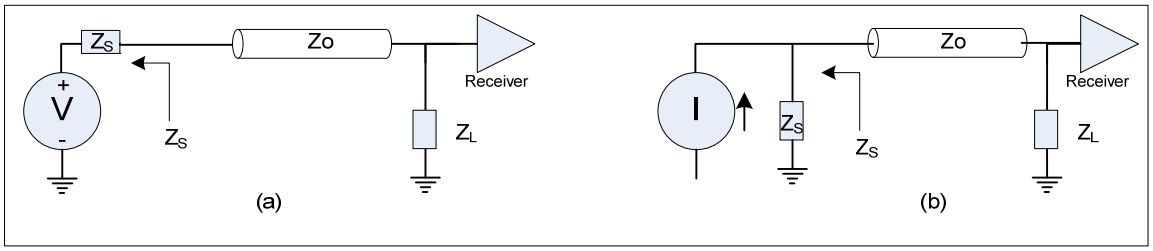


Figure 26: Double termination technique

In some applications it may be difficult to reduce load or source reflection coefficients to acceptably small values, e.g., due to the excessive parasitic capacitances and inductances. Terminating at both ends of the transmission line is an effective way to reduce round-trip reflection and improve signal integrity. Figure 26 shows double termination for voltage and current drivers. For example, if $\Gamma_L = \Gamma_S = 0.1$, then $\Gamma_{RT} = 0.01$, i.e., only 1% of the signal reflect back to the load.

One drawback of double termination is that the effective signal reaching the load will be half of the signal in load- or source-only terminated circuits. Drivers that can provide twice the nominal drive are attractive solutions to signal integrity problems using the double termination strategy. The additional drive causes more power consumption in the load and source terminations, but overall power consumption goes up only marginally in cases where the load power consumption is small relative to that of the driver.

SiTime Corporation
990 Almanor Avenue
Sunnyvale, CA 94085
USA
Phone: 408-328-4400
http://www.sitime.com